

CLAIMS

What is claimed is:

1. A flip-flop circuit comprising:

a single-input tri-state inverter for receiving an input D;

a dual-input inverter;

a first and second single-event transient (SET) filters;

a dual-input tri-state inverter includes a first input for receiving output signals from said dual-input inverter, a second input for receiving output signals from said dual-input inverter via said first SET filter, and an output for sending output signals to a first input of said dual-input inverter and to a second input of said dual-input inverter via said second SET filter; and

a single-input inverter for receiving inputs from said dual-input inverter to provide an output Q for said flip-flop circuit.

2. The flip-flop circuit of Claim 1, wherein said dual-input inverter includes a p-channel transistor and an n-channel transistor connected in series between power and ground.
3. The flip-flop circuit of Claim 1, wherein said dual-input inverter includes two p-channel transistors and two n-channel transistors connected in series between power and ground.
4. The flip-flop circuit of Claim 1, wherein said dual-input tri-state inverter includes a dual-input inverter and a transmission gate.
5. The flip-flop circuit of Claim 1, wherein said dual-input tri-state inverter includes two p-channel transistors and two n-channel transistors connected in series between power and ground.
6. The flip-flop circuit of Claim 1, wherein said first SET filter includes two inverters connected in series and a capacitor connected between said two inverters.
7. The flip-flop circuit of Claim 6, wherein said second SET filter includes two inverters connected in series and a capacitor connected between said two inverters.

8. A flip-flop circuit comprising:

a first single-input tri-state inverter for receiving an input D;

a first dual-input inverter;

a first and second single-event transient (SET) filters;

a first dual-input tri-state inverter includes a first input for receiving output signals from said first dual-input inverter, a second input for receiving output signals from first said dual-input inverter via said first SET filter, and an output for sending output signals to a first input of said first dual-input inverter and to a second input of said first dual-input inverter via said second SET filter;

a second single-input tri-state inverter for receiving output from said first dual-input inverter;

a second dual-input inverter;

a third and fourth SET filters; and

a second dual-input tri-state inverter includes a first input for receiving output signals from said second dual-input inverter, a second input for receiving output signals from said second dual-input inverter via said third SET filter, and an output for sending output signals to a first input of said second dual-input inverter and to a second input of said second dual-input inverter via said fourth SET filter, wherein said second dual-input inverter provides an output Q for said flip-flop circuit.

9. The flip-flop circuit of Claim 8, wherein said first dual-input inverter includes a p-channel transistor and an n-channel transistor connected in series between power and ground.
10. The flip-flop circuit of Claim 8, wherein said first dual-input inverter includes two p-channel transistor and two n-channel transistors connected in series between power and ground.
11. The flip-flop circuit of Claim 8, wherein said second dual-input inverter includes a p-channel transistor and an n-channel transistor connected in series between power and ground.
12. The flip-flop circuit of Claim 8, wherein said second dual-input inverter includes two p-channel transistor and two n-channel transistors connected in series between power and ground.
13. The flip-flop circuit of Claim 8, wherein said first dual-input tri-state inverter includes a dual-input inverter and a transmission gate.
14. The flip-flop circuit of Claim 8, wherein said first dual-input tri-state inverter includes two p-channel transistors and two n-channel transistors connected in series between power and ground.
15. The flip-flop circuit of Claim 8, wherein said second dual-input tri-state inverter includes a dual-input inverter and a transmission gate.
16. The flip-flop circuit of Claim 8, wherein said second dual-input tri-state inverter includes two p-channel transistors and two n-channel transistors connected in series between power and ground.
17. The flip-flop circuit of Claim 8, wherein said first SET filter includes two inverters connected in series and a capacitor connected between said two inverters.
18. The flip-flop circuit of Claim 17, wherein said second SET filter includes two inverters connected in series and a capacitor connected between said two inverters.

19. The flip-flop circuit of Claim 18, wherein said third SET filter includes two inverters connected in series and a capacitor connected between said two inverters.
20. The flip-flop circuit of Claim 19, wherein said fourth SET filter includes two inverters connected in series and a capacitor connected between said two inverters.