ARRAY DATA BIT INVERSION

CROSS-REFERENCES

[0001] The present Application for Patent claims priority to PCT Application No. PCT/US2017/035452, entitled "Array Data Bit Inversion," filed June 1, 2017, which claims priority to U.S. Patent Application No. 15/188,890 by Ingalls et al., entitled "Array Data Bit Inversion," filed June 21, 2016, assigned to the assignee hereof and each of which is expressly incorporated by reference in its entirety herein.

BACKGROUND

[0002] The following relates generally to memory devices and more specifically to maintaining the performance of ferroelectric memory cells that store logic values for extended periods of time.

[0003] Memory devices are widely used to store information in various electronic devices such as computers, wireless communication devices, cameras, digital displays, and the like. Information is stored by programing different states of a memory device. For example, binary devices have two states, often denoted by a logic "1" or a logic "0." In other systems, more than two states may be stored. To access the stored information, the electronic device may read, or sense, the stored state in the memory device. To store information, the electronic device may write, or program, the state in the memory device.

[0004] Various types of memory devices exist, including random access memory (RAM), read only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, and others. Memory devices may be volatile or non-volatile. Non-volatile memory (e.g., flash memory) can store data for extended periods of time even in the absence of an external power source. Volatile memory devices (e.g., DRAM) may lose their stored state over time unless they are periodically refreshed by an external power source. A binary memory device may, for example, include a charged or discharged capacitor. A charged capacitor may, however, become discharged over time through leakage currents, resulting in the loss of the stored information. Certain features of volatile memory may offer performance advantages, such as faster read or write speeds, while features of non-volatile memory, such as the ability to store data without periodic refreshing, may be advantageous.

[0005] FeRAM may use similar device architectures as volatile memory but may have non-volatile properties due to the use of a ferroelectric capacitor as a storage device. FeRAM devices may thus have improved performance compared to other non-volatile and volatile

[0020] In some cases, the additional logic used to read the originally stored or intended logic state may be implemented in a manner that is not communicated to the other sensing components. That is, a value indicating whether an intended or different logic state being stored by the cell may not be provided to the sense component or to the ECC logic. In some examples, a first and second set of transistors may be configured around a sense component such that the first set of transistors, which may be referred to as "true transistors," may be used to read or write a true logic state from or to the cell—e.g., if the read logic state is the same as the stored logic state. And the second set of transistors, which may be referred to as the "inverting transistors," may be used to read or write a different logic state from the logic state stored by or intended for the cell—e.g., the read logic state is the opposite of the stored logic state. The true transistors or the inverting transistors may be activated based on whether the intended logic state or an inverted logic state is stored by or is to be written to the cell. So, whether a cell is accessed through the true transistors or the inverting transistors may depend on whether the cell is presently storing the intended or inverted state.

[0021] In some cases, the true transistors may be used to read and write-back the logic state stored by the cell if the logic state is the intended logic state, while the inverting transistors may be used to read and write-back the logic state stored by the cell if the logic state is the inverted logic state. In this way, the sense component (e.g., a sense amplifier) may generate a voltage corresponding to the intended logic state based on the signals that are sensed at the inputs of the sense component without having to determine whether or not to change the resulting voltage to reflect the intended logic state. In some examples, a logic state stored by the cell may be read using the true transistors and the inverted logic state may be written-back to the cell using the inverting transistors. So, the inverted logic state may be re-written to the cell without a sense component having to change the voltage resulting from the sensing operation to a different voltage.

[0022] In some examples, a counter may be used to determine which of the first set of transistors and the second set of transistors to use for a read or write operation. For instance, the logic states stored by cells of an array may be sequentially inverted and a value of a counter may be concurrently updated with the inversion to reflect the address of the last cell to be updated. The value of the counter may be used to determine whether a cell that is to be accessed (e.g., read or written) is expected to be storing an intended logic state or an inverted

[0030] Upon accessing, a memory cell 105 may be read, or sensed, by sense component 125 to determine the stored state of the memory cell 105. For example, after accessing the memory cell 105, the ferroelectric capacitor of memory cell 105 may discharge onto its corresponding digit line 115. Discharging the ferroelectric capacitor may be based on biasing, or applying a voltage, to the ferroelectric capacitor. The discharging may induce a change in the voltage of the digit line 115, which sense component 125 may compare to a reference voltage (not shown) in order to determine the stored state of the memory cell 105. For example, if digit line 115 has a higher voltage than the reference voltage, then sense component 125 may determine that the stored state in memory cell 105 was a logic 1 and vice versa.

[0031] The reliability of a sensing operation may be dependent on a sensing window that results from reading the memory cell 105. For instance, a larger sensing window may be associated with fewer bit errors than a smaller sensing window. The sensing window may be determined as the difference between a voltage of a digit line 115 resulting from reading a memory cell 105 when storing a logic 1 and the voltage of the digit line 115 resulting from reading the memory cell when storing a logic 0. Sense component 125 may include various transistors or amplifiers in order to detect and amplify a difference in the signals, which may be referred to as latching. The detected logic state of memory cell 105 may then be output through column decoder 130 as output 135.

[0032] A memory cell 105 may be set, or written, by activating the relevant word line 110 and digit line 115. As discussed above, activating a word line 110 electrically connects the corresponding row of memory cells 105 to their respective digit lines 115. By controlling the relevant digit line 115 while the word line 110 is activated, a memory cell 105 may be written—i.e., a logic value may be stored in the memory cell 105. Column decoder 130 may accept data, for example input 135, to be written to the memory cells 105. A ferroelectric memory cell 105 may be written by applying a voltage across the ferroelectric capacitor. This process is discussed in more detail below.

[0033] In some memory architectures, accessing the memory cell 105 may degrade or destroy the stored logic state and re-write or refresh operations may be performed to return the original logic state to memory cell 105. In DRAM, for example, the capacitor may be partially or completely discharged during a sense operation, corrupting the stored logic state. So, the logic state may be re-written after a sense operation. Additionally, activating a single

array 100 with a logic state opposite the currently stored logic state (e.g., the inverted logic state) and opposite the logic state intended to be read from the ferroelectric memory cell. For instance, the memory controller 140 may identify a time period (e.g., a time period that corresponds to a point in time at which the expected sensing window falls below a threshold value after storing an initial value) and may update one or more ferroelectric memory cells 105 of the memory array 100 according to the identified period of time. In some cases, the time period may be determined based on internal characteristics of the ferroelectric memory cells 105, a temperature of the memory array 100, an age of the ferroelectric memory cells 105, a sensing window resulting from reading the ferroelectric memory cells 105, or the like.

[0037] Additional logic may be used to invert a logic state of a memory cell so that the memory controller 140 (or other components of or using the memory array 100) is aware which ferroelectric memory cells 105 are storing intended logic states and which ferroelectric memory cells 105 are storing inverted logic states. In some examples, one or more indicators may be associated with one or more memory and values of the indicators may be used to indicate whether the memory cells are storing intended or inverted logic states.

[0038] By way of example, a value of “0” may indicate that the intended logic state is stored, while a value “1” may indicate that the inverted logic state is stored. This value may be provided to sense component 125, which may use the value to maintain or invert a voltage generated by the sense component 125 after performing a sensing operation. For instance, if a memory cell 105 is storing an inverted logic state 0, a negative voltage may be generated across the sense component 125, where the positive terminal is associated with the digit line 115 and the negative terminal is associated with the reference line (i.e., the digit line 115 may be at a lower voltage than the reference line), after a sense operation is performed. The sense component 125 may then invert the voltage so that a positive voltage, corresponding to an intended logic state 1, is applied across the sense component based on receiving a value “1” from the indicator.

[0039] In some case, processing the indicator value at the sense component 125 to determine the proper voltage to output—e.g., the voltage corresponding to the intended or inverted logic state—may result in increased latency, undesirable modifications to the sense component, or an increased likelihood of error in a read operation. For example, the sense component 125 may be modified from other architectures to accommodate the indicator value, and at times the indicator value may be incorrect. Furthermore, if ECC logic is used,

similar modifications may be needed to accommodate the indicator value. In order to avoid physical or operational modifications to sensing components, such as sense component 125 or ECC logic, additional components may be placed around the sense component 125 such that the sense component may output the intended or inverted logic states with no or little additional processing. For example, a first set of transistors, or "true transistors," may be used to read the logic state currently stored by a ferroelectric memory cell 105 and a second set of transistors, or "inverting transistors," may be used to read a logic state opposite than that stored by the ferroelectric memory cell 105. The true and inverting transistors may be strategically activated for access operations based on whether or not an intended logic state is stored by the ferroelectric memory cell 105. In some examples, activating the true and inverting transistors is based on an address associated with the ferroelectric memory cell 105 and a value of a counter used to indicate an address of the last group of memory cells that is storing inverted logic state.

[0040] The memory controller 140 may control the operation (e.g., read, write, re-write, refresh, etc.) of memory cells 105 through the various components, such as row decoder 120, column decoder 130, and sense component 125. Memory controller 140 may generate row and column address signals in order to activate the desired word line 110 and digit line 115. Memory controller 140 may also generate and control various voltage potentials used during the operation of memory array 100. In general, the amplitude, shape, or duration of an applied voltage discussed herein may be adjusted or varied and may be different for the various operations for operating memory array 100. Furthermore, one, multiple, or all memory cells 105 within memory array 100 may be accessed simultaneously; for example, multiple or all cells of memory array 100 may be accessed simultaneously during a reset operation in which all memory cells 105, or a group of memory cells 105, are set to a single logic state.

[0041] In some cases, the memory controller 140 may be used to maintain the performance of a ferroelectric memory cell 105. For example, memory controller 140 may be used to activate either the true transistors or the inverting transistors when accessing one or more ferroelectric memory cells 105. In some examples, the memory controller 140 may activate the true transistors to read a logic state stored by the ferroelectric memory cells 105 and may subsequently activate the inverting transistors to write the opposite logic state to the ferroelectric memory cells 105. In this way, the memory controller 140 may invert a logic

positive voltage, voltage 335 may be negative. In response to voltage 335, charge state 305-b may follow path 340. Likewise, if charge state 310-b was initially stored, then it follows path 345. The final position of charge state 305-c and charge state 310-c depend on a number of factors, including the specific sensing scheme and circuitry.

[0060] In some cases, the final charge may depend on the intrinsic capacitance of the digit line connected to the memory cell. For example, if the capacitor is electrically connected to the digit line and voltage 335 is applied, the voltage of the digit line may rise due to its intrinsic capacitance. So, a voltage measured at a sense component may not equal voltage 335 and instead may depend on the voltage of the digit line. The position of final charge states 305-c and 310-c on hysteresis curve 300-b may thus depend on the capacitance of the digit line and may be determined through a load-line analysis—i.e., charge states 305-c and 310-c may be defined with respect to the digit line capacitance. As a result, the voltage of the capacitor, voltage 350 or voltage 355, may be different and may depend on the initial state of the capacitor.

[0061] By comparing the digit line voltage to a reference voltage, the initial state of the capacitor may be determined. The digit line voltage may be the difference between voltage 335 and the final voltage across the capacitor, voltage 350 or voltage 355—i.e., (voltage 335 – voltage 350) or (voltage 335 – voltage 355). A reference voltage may be generated so that its magnitude is between the two possible digit line voltages in order to determine the stored logic state—i.e., to determine whether the digit line voltage is higher or lower than the reference voltage. For example, the reference voltage may be an average of the two quantities, (voltage 335 – voltage 350) and (voltage 335 – voltage 355). Upon comparison by the sense component, the sensed digit line voltage may be determined to be higher or lower than the reference voltage, and the stored logic value of the ferroelectric memory cell (i.e., a logic 0 or 1) may be determined.

[0062] As discussed above, reading a memory cell that does not use a ferroelectric capacitor may degrade or destroy the stored logic state when the cell is read. A ferroelectric memory cell, however, may maintain the initial logic state after a read operation. For example, if charge state 310-b is stored, the charge state may follow path 345 to charge state 310-c during a read operation and after applying voltage 350. In some cases, reading a ferroelectric memory cell may disturb the logic state of the cell. For instance, charge state 310-b may no longer be stored after reading the ferroelectric memory cell. Therefore, a write-

[0065] Multiple sets of transistors may be used for writing back an opposite logic state and for reading an intended logic state from a ferroelectric memory cell. For instance, a first set of transistors may be configured around a sense component to enable the reading/writing of the true logic states from/to a ferroelectric memory cell. And a second set of transistors may be configured around a sense component for reading an intended logic state from a ferroelectric capacitor storing an inverted logic state. Additionally, the second set of transistors may be used to write an inverted logic state to a ferroelectric memory cell that is expected to be storing an inverted logic state.

[0066] **FIG. 4A** illustrates an example circuit 400-a that supports the inversion of data bits in accordance with various embodiments of the present disclosure. Circuit 400-a includes memory cells 105-b and 105-c, word line 110-b (which may also be referred to as an access line), digit line 115-b, and sense component 125-b, which may be examples of a memory cell 105, word line 110, digit line 115, and sense component 125, respectively, described with reference to FIG. 1 and 2. Memory cells 105-b and 105-c may include a ferroelectric capacitor that operates with characteristics as described with reference to FIG. 3. Circuit 400-a also includes plate line 210-a and reference line 225-a, which may be examples of plate line 210 and reference line 225, respectively, described with reference to FIG. 2. Circuit 400-a also includes voltage source 405, voltage source 410, equalization switches 420-a and 420-b, and isolation components 425-a and 425-b. Equalization switches 420 and isolation components 425 may also be generally referred to as switching components.

[0067] Digit line 115-b and reference line 225-a may have intrinsic capacitances 415-a and 415-b, respectively. Intrinsic capacitances 415-a and 415-b may not be electrical devices—i.e., they may not be two-terminal capacitors. Instead, intrinsic capacitances 415-a and 415-b may represent capacitance that results from physical characteristics, including the dimensions, of digit line 115-b and reference line 225-a. In some cases, reference line 225-a is an unused or inactive digit line. In some examples, digit line 115-b and reference line 225-a may be connected to or separated from virtual ground through equalization switches 420-a and 420-b. A virtual ground may act as a common reference for circuit 400-a and may also be referred to as ground or 0V, although, the virtual ground may float to a voltage that is different than (e.g., greater or less than) zero volts when compared with an earth ground.

[0068] In some examples, control signals (e.g., a linear equalization signal) may be used to activate or deactivate equalization switches 420-a or 420-b by increasing or decreasing a

other types of memory cells (e.g., DRAM, memory-RAM (MRAM), etc.). For instance, the true isolation components 425-a and the inverting isolation components 425-b may similarly be used to read and/or store intended or inverted logic states to or from the other types of memory cells.

[0080] **FIG. 4B** illustrates an example operation of circuit 400-b where true isolation components 425-a are activated and inverting isolation components 425-b are deactivated in accordance with various embodiments of the present disclosure. For ease of reference, the deactivated inverted isolation components 425-b and second ferroelectric memory cell 105-c are not drawn in circuit 400-b. As shown in FIG 4B, activating true isolation components 425-a-1 and 425-a-2 provides a conductive path between first input line 240-c and digit line 115-b and another conductive path between second input line 240-d and reference line 225-a. This configuration may result in sense component 125-b outputting a voltage that corresponds to the logic state that is currently stored by memory cell 105-d (i.e., the true logic state). For example, if memory cell 105-d stores a logic value 1, sense component 125-b will output a voltage corresponding to the logic value 1. This configuration may be used to access a memory cell that does not store an inverted logic state.

[0081] **FIG. 4C** illustrates an example operation of circuit 400-c where true isolation components 425-a are deactivated and inverting isolation components 425-b are activated in accordance with various embodiments of the present disclosure. For ease of reference, the deactivated true isolation components 425-a and second ferroelectric memory cell 105-c are not drawn in circuit 400-c. As shown in FIG 4C, activating inverting isolation components 425-b-1 and 425-b-2 provides a conductive path between first input line 240-c and reference line 225-a and another conductive path between second input line 240-d and digit line 115-b. This configuration may result in sense component 125-b outputting a voltage that corresponds to a logic state that is opposite the logic state that is currently stored by memory cell 105-e (i.e., the inverted logic state). For example, if memory cell 105-e stores a logic value 1, sense component 125-b will output a voltage corresponding to the logic value 0.

[0082] This configuration may be used to access a memory cell that is storing or is expected to be storing an inverted logic state. For instance, the controller may determine that an address used to access memory cell 105-e is selected for a write operation. The controller may also determine the address to be accessed is less than the address associated with the counter and may determine that an inversion operation has been performed for the page and

sensing voltage resulting from reading a memory cell, such as first ferroelectric memory cell 105-b may be represented as a function of time. Timing diagram 500-b depicts an example operation of circuit 400 described with reference to FIGs. 4A-4C. FIG. 5B is described below with reference to components of preceding figures. FIG. 5B may illustrate aspects of a data inversion operation for a memory cell, during which a read operation is performed using true isolation components 425-a and a write-back operation is performed using inverting isolation components 425-b. The read operation may correspond to the configuration provided in circuit 400-b, while the write-back operation may correspond to the configuration provided in circuit 400-c. The operation discussed in FIG. 5C may be used to invert and un-invert (i.e., return to true) logic states stored by memory cells.

[0092] As discussed with reference to FIGs. 4A-4C and 5A, first ferroelectric memory cell 105-b may be read using true isolation components 425-a. Similar to the read operation performed in FIG 5A, the gut voltage 535-a may result if first ferroelectric memory cell 105-b originally stores a logic 1, while gut voltage 535-b may result if first ferroelectric memory cell 105-b originally stores a logic 0. Accordingly, the memory controller may read the true logic state of first ferroelectric memory cell 105-b based on the output voltage of sense component 125-b. Although in some cases, the memory controller may refrain from reading a logic state during an inversion operation. However, after storing the output the write back operation may be performed using inverting isolation components 425-b. That is, true isolation voltage 515-c may be maintained at or near virtual ground, while inverting isolation voltage 515-d may be increased to activate inverting isolation components 425-b. As a result, the voltage of second input line 240-d may be applied to digit line 115-b for the write-back operation.

[0093] As discussed above the voltage of second input line 240-d moves opposite the gut voltage 535. Accordingly, after electrically returning sense component 125-b to circuit 400, the digit line voltage 530 may not follow the corresponding gut voltage 535 but may follow the complementary gut voltage. Therefore, the digit line voltage 530 used to write the sensed logic state back to first ferroelectric memory cell 105-b may be associated with the opposite logic state and the first ferroelectric memory cell 105-b may store an inverted logic state. For example, first ferroelectric memory cell 105-b may originally store a logic 1 and digit line voltage 530-a may result when first ferroelectric memory cell 105-b is accessed (e.g., by asserting word line voltage 525). True isolation components 425-a may be used to read first

voltages 535-a and 535-b being measured at first input line 240-c. Concurrently, the voltage of second input line 240-c may be driven to high voltage source 405.

[0100] Otherwise, if digit line voltage 530-b is present on digit line 115-b, the gut voltage 535-b may be driven to high voltage source 405, and the voltage of second input line 240-d may be driven to low voltage source 410. Since digit line 115-b may be isolated from the gut of sense component 125-b, the resulting digit line voltages 530 may be maintained throughout the comparison. The output voltage of sense component 125-b (e.g., output voltage = the voltage of first input line 240-c – the voltage of second input line 240-d) may be stored in a latch and read by a memory controller to determine the corresponding logic state stored by first ferroelectric memory cell 105-b. Accordingly, the output voltage of sense component 125-b may correspond to a logic state opposite the logic state stored by memory cell 105-b. For instance, the memory controller may determine that first ferroelectric memory cell 105-b originally stored a logic state 0 if gut voltage 535-a is a low voltage (e.g., virtual ground), despite memory cell originally storing a logic state 1.

[0101] After storing the output voltage of sense component 125-b, inverting isolation voltage 515-d may be reapplied to inverting isolation components 425-b electronically returning sense component 125-b back into circuit 400 and providing a conductive path between digit line 115-b and second input line 240-d. Reconnecting the digit line 115-b to second input line 240-d may result in the digit line voltage 530 being driven to a voltage opposite the resulting gut voltage 535-a at first input line 240-c. For instance, if first ferroelectric memory cell 105-b originally stores a logic state 1, the corresponding digit line voltage 530-a may rise to a complementary voltage to gut voltage 535-a (since gut voltage 535-a is measured at first input line 240-c and digit line 115-b is connected to second input line 240-d). Or if first ferroelectric memory cell 105-b originally stores a logic state 0, the corresponding digit line voltage 530-b may decrease to the complementary voltage to gut voltage 535-b.

[0102] Therefore, the digit line voltage 530 used to write the sensed logic state back to first ferroelectric memory cell 105-b may be associated with the opposite logic state and the first ferroelectric memory cell 105-b may store an inverted logic state. For example, first ferroelectric memory cell 105-b may originally store a logic 1 and digit line voltage 530-a may result when first ferroelectric memory cell 105-b is accessed (e.g., by asserting word line voltage 525). Inverting isolation components 425-a may be used to read first ferroelectric

CLAIMS

What is claimed is:

1. A method, comprising:

applying a first voltage across a memory cell;

deactivating a first transistor that is in electronic communication with a first input of a sense component and the memory cell based at least in part on applying the first voltage;

activating the sense component based at least in part on deactivating the first transistor;

activating a second transistor that is in electronic communication with a second input of the sense component and the memory cell based at least in part on activating the sense component; and

applying a second voltage across the memory cell based at least in part on activating the second transistor.

2. The method of claim 1, further comprising:

applying a third voltage across a reference cell; and

deactivating a third transistor that is in electronic communication with the second input of the sense component and the reference cell based at least in part on applying the first voltage across the memory cell and applying the third voltage across the reference cell.

3. The method of claim 2, further comprising:

activating a fourth transistor that is in electronic communication with the first input of the sense component and the reference cell based at least in part on activating the sense component.

4. The method of claim 1, wherein applying the second voltage across the memory cell comprises:

applying a third voltage to a bit line that is in electronic communication with the memory cell via the second transistor, the third voltage comprising a voltage at the second input of the sense component based at least in part on activating the sense component; and

applying a fourth voltage to a plate line that is in electronic communication with the memory cell during an overlapping time period with applying the third voltage.

5. The method of claim 1, wherein applying the first voltage across the memory cell comprises:

applying a third voltage to a selection component that is in electronic communication with a storage component of the memory cell and a bit line that is in electronic communication with the memory cell and the first transistor; and

applying a fourth voltage to a plate line that is in electronic communication with the memory cell.

6. The method of claim 1, wherein the memory cell stores a first logic state before the first voltage is applied and stores a second logic state, different than the first logic state, after the second voltage is applied.

7. The method of claim 6, further comprising:

applying a third voltage across the memory cell after applying the second voltage;

deactivating the first transistor that is in electronic communication with the first input of the sense component and the memory cell based at least in part on applying the first voltage across the memory cell;

activating the sense component based at least in part on deactivating the first transistor;

activating the second transistor that is in electronic communication with the second input of the sense component and the memory cell based at least in part on activating the sense component; and

applying a fourth voltage across the memory cell based at least in part on activating the second transistor, wherein the memory cell stores the first logic state after the fourth voltage is applied.

8. The method of claim 6, further comprising:

performing a read operation of the memory cell after applying the second voltage, wherein reading the memory cell comprises deactivating the first transistor and

activating the second transistor for the read operation based at least in part on the memory cell storing the second logic state.

9. The method of claim 1, further comprising:

updating a value of a counter based at least in part on activating the second transistor, wherein the value of the counter is associated with an address used for accessing the memory cell.

10. The method of claim 9, further comprising:

comparing the value of the counter with the address used for accessing the memory cell; and

performing a read operation of the memory cell after applying the second voltage, wherein reading the memory cell comprises deactivating the first transistor and activating the second transistor for the read operation based at least in part on the comparison of the value of the counter with the address.

11. An apparatus, comprising:

a bit line;

a reference bit line;

a sense component comprising a first input line and a second input line;

a first transistor in electronic communication with and between the bit line and the first input line of the sense component;

a second transistor in electronic communication with and between the bit line and the second input line of the sense component;

a third transistor in electronic communication with and between the reference bit line and the first input line of the sense component; and

a fourth transistor in electronic communication with and between the reference bit line and the second input line of the sense component.

12. The apparatus of claim 11, further comprising:

a ferroelectric memory cell in electronic communication with the bit line.

13. The apparatus of claim 11, wherein:

the first transistor, the second transistor, and the bit line share a first common node, the first transistor being physically or electrically between the first common node and

the first input line of the sense component and the second transistor being physically or electrically between the first common node and the second input line of the sense component; and

the third transistor, the fourth transistor, and the reference bit line share a second common node, the third transistor being physically or electrically between the second common node and the first input line of the sense component and the fourth transistor being physically or electrically between the second common node and the second input line of the sense component.

14. The apparatus of claim 11, wherein the first transistor, the second transistor, the third transistor, and the fourth transistor are external to the sense component.

15. An apparatus, comprising:

an access line;

a reference line;

a sense component comprising a first input line and a second input line;

a first transistor in electronic communication with the access line and the first input line of the sense component;

a second transistor in electronic communication with the access line and the second input line of the sense component;

a third transistor in electronic communication with the reference line and the first input line of the sense component;

a fourth transistor in electronic communication with the reference line and the second input line of the sense component;

a first set of control lines in electronic communication with the first transistor and the second transistor;

a second set of control lines in electronic communication with the third transistor and the second transistor; and

a counter in electronic communication with the first set of control lines and the second set of control lines.

16. The apparatus of claim 15, wherein the counter comprises a non-volatile latch.

17. An apparatus, comprising:

a memory cell;

a sense component;

a first transistor in electronic communication a first input of the sense component and the memory cell;

a second transistor in electronic communication with a second input of the sense component and the memory cell; and

a controller in electronic communication with the memory cell, the first transistor, the second transistor, and the sense component, wherein the controller comprises code executable to cause the apparatus to:

deactivate the first transistor in response to a first voltage being applied to the memory cell;

activate the sense component in response to deactivating the first transistor;

activate the second transistor in response to activating the sense component; and

apply a second voltage to the memory cell based at least in part on activating the second transistor.

18. The apparatus of claim 17, wherein the code is further executable to cause the apparatus to:

apply the first voltage to the memory cell, wherein the first transistor is in an active state when the first voltage is applied; and

apply a third voltage to the memory cell based at least in part on activating the first transistor.

19. The apparatus of claim 17, further comprising:

a reference cell;

a third transistor that is in in electronic communication with the second input of the sense component and the reference cell, wherein the code is further executable to cause the apparatus to:

apply a third voltage to the reference cell; and

deactivate the third transistor in response to the first voltage being applied to the memory cell and applying the third voltage across the reference cell.

20. The apparatus of claim 19, further comprising:

a fourth transistor that is in electronic communication with the first input of the sense component and the reference cell, wherein the code is further executable to cause the apparatus to:

activate the fourth transistor in response to activating the sense component.

21. The apparatus of claim 17, further comprising:

a counter, wherein the code is further executable to cause the apparatus to:

update a value of the counter in response to activating the second transistor, wherein the value of the counter is associated with an address used for accessing the memory cell.