

ABSTRACT

An apparatus for performing a scan test of an integrated-circuit (IC) chip including a test target circuit, a scan input port, and a scan output port, by inputting a scan pattern to a scan path via the scan input port and comparing an output value outputted via the scan output port with a predetermined expected value includes a shift-frequency searching unit configured to search a shift frequency with which a result of the scan test indicates a pass or a shift frequency with which the result of the scan test indicates a fail, by shifting, to the scan path, a target scan section for which a usable shift frequency is to be searched from among two or more scan sections included in a scan pattern set. When searching the shift frequency for the target scan section, the shift-frequency searching unit is configured to search a shift frequency with which the result of the scan test indicates the pass or a shift frequency with which the result of the scan test indicates the fail, by scaling the shift frequency of the target scan section differently from that of at least one scan section among other scan sections shifted to the scan path or by setting the shift frequency of the target scan section differently from that of at least one scan section among the other scan sections shifted to the scan path.

Figure 12