WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a substrate;

at least one first chip on an upper surface of the substrate;

a second chip on the upper surface of the substrate and located beside the at least one first chip as viewed in a plan view; and

a support structure on the second chip,

wherein a width of the support structure, in a direction parallel to the upper surface of the substrate, is greater than a width of the second chip in said direction.

2. The semiconductor package of claim 1, wherein a distance from the upper surface of the substrate to a top surface of the support structure is substantially the same as a distance from the upper surface of the substrate to a top surface of an uppermost one of the at least one first chip.

3. The semiconductor package of claim 1, wherein the support structure comprises a block of insulating material, a dummy chip, or a memory chip.

4. The semiconductor package of claim 1, wherein the support structure comprises silicon (Si).

5. The semiconductor package of claim 1, wherein each said at least one first chip is a memory chip, and

the second chip is a logic chip.

6. The semiconductor package of claim 1, wherein the at least one first chip is wire-bonded to the substrate, and

the second chip is flip-chip bonded to the substrate.

7. The semiconductor package of claim 5, wherein the at least one first chip comprises a stack of first chips.

8. The semiconductor package of claim 1, further comprising at least one third chip on the at least one first chip and the second chip.

9. The semiconductor package of claim 1, further comprising at least one third chip on the at least one first chip and the support structure.

10. The semiconductor package of claim 8, further comprising a first spacer interposed between the at least one first chip and the at least one third chip.

11. The semiconductor package of claim 10, further comprising at least one fourth chip on the upper surface of the substrate and disposed beside the at least one first chip and the second chip as viewed in a plan view, the at least one fourth chip being interposed between substrate and the first spacer.

12. The semiconductor package of claim 11, wherein the at least one first

chip comprises a stack of first chips and/or the at least one fourth chip comprises a stack of fourth chips.

13. The semiconductor package of claim 11, wherein the at least one third chip includes a stack of third chips, and

the semiconductor package further comprises a second spacer disposed in the stack of third chips between respective groups of the third chips.

14. The semiconductor package of claim 11, wherein each said at least one fourth chip is a memory chip.

15. A semiconductor package, comprising:

a substrate;

at least one first chip disposed on and wire-bonded to the substrate;

a second chip disposed on the substrate beside the at least one first chip as viewed in a plan view and flip-chip bonded to the substrate;

at least one third chip disposed on as spanning the at least one first chip and the second chip;

a first spacer interposed between the at least one first chip and the second chip, collectively, and the at least one third chip; and

a support structure interposed between the second chip and the first spacer,

wherein a width of the support structure, in a direction parallel to an upper surface of the substrate, is greater than a width of the second chip in said direction.

16. The semiconductor package of claim 15, wherein each said at least one first chip is a memory chip, and the second chip is a logic chip.

17. The semiconductor package of claim 15, wherein the at least one third chip comprises a plurality of memory chips.

18. The semiconductor package of claim 15, further comprising at least one fourth chip disposed on the substrate beside the at least one first chip and the second chip as viewed in a plan view, the at least one fourth chip being interposed between the substrate and the first spacer.