FIG. 1A

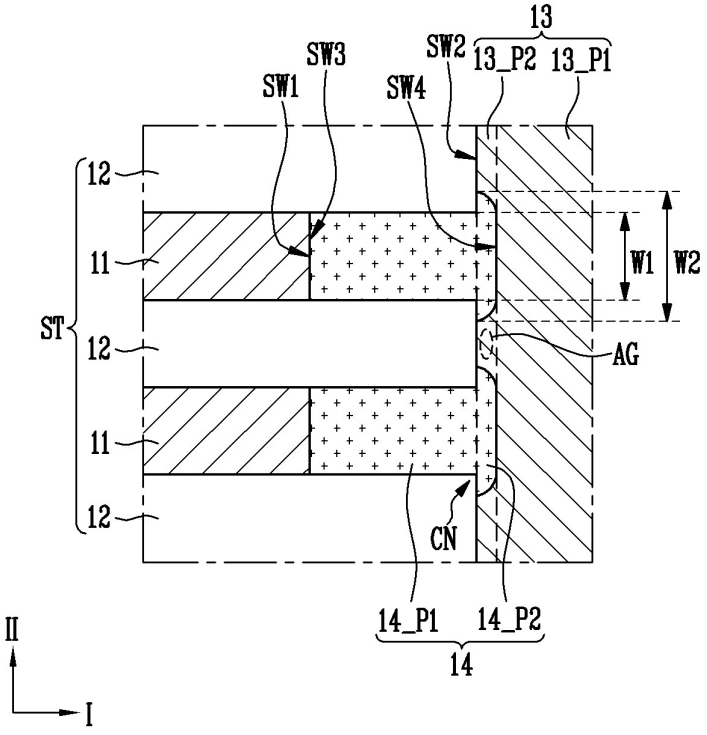

13
SW2
SW3
13_P2
13_P1
SW1
SW4
12
11
W1
W2
ST
12
AG
11
12
CN
14_P1
14_P2
14
II
I

FIG. 1B

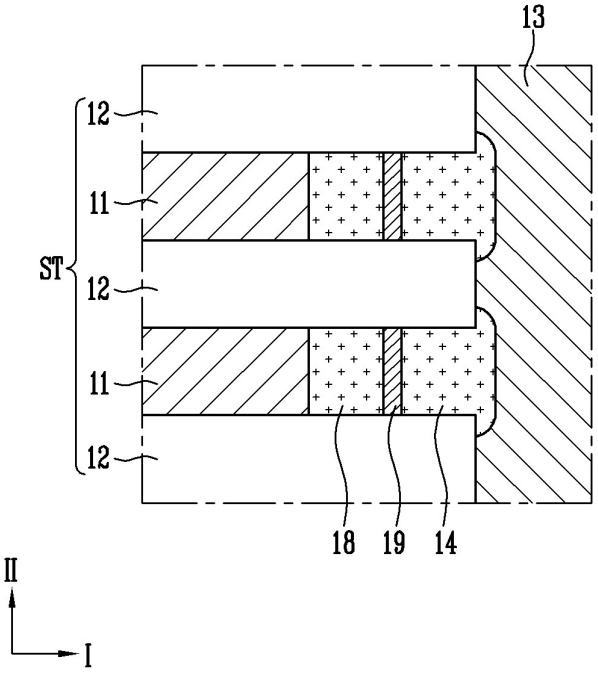


FIG. 2

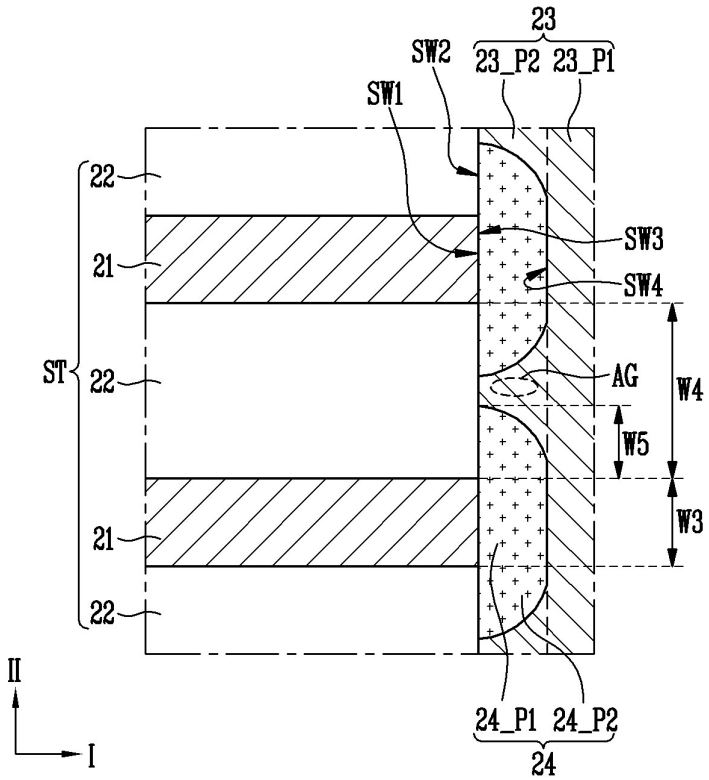

23
SW2
23_P2
23_P1
SW1
22
21
SW3
SW4
ST
22
AG
W4
W5
21
W3
22
II
I
24_P1
24_P2
24

FIG. 3A

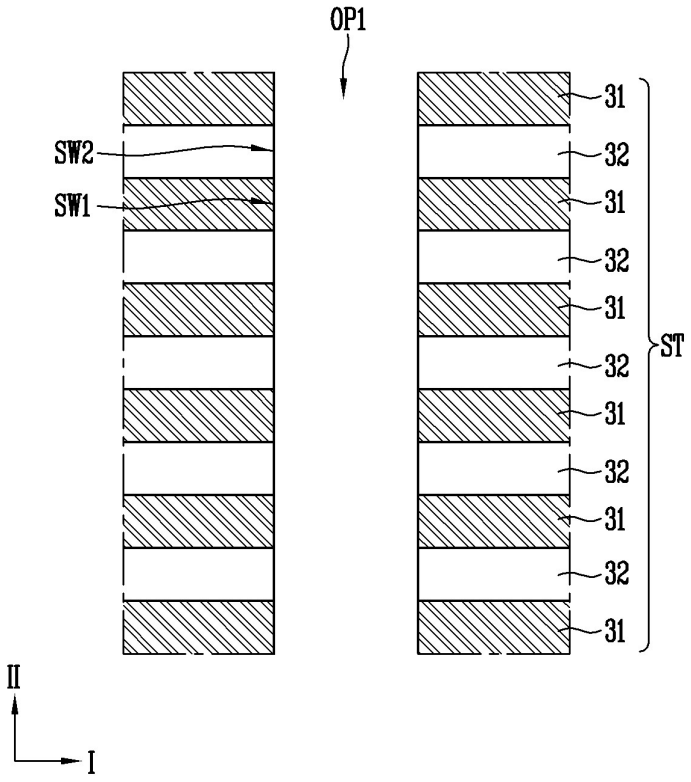


FIG. 3B

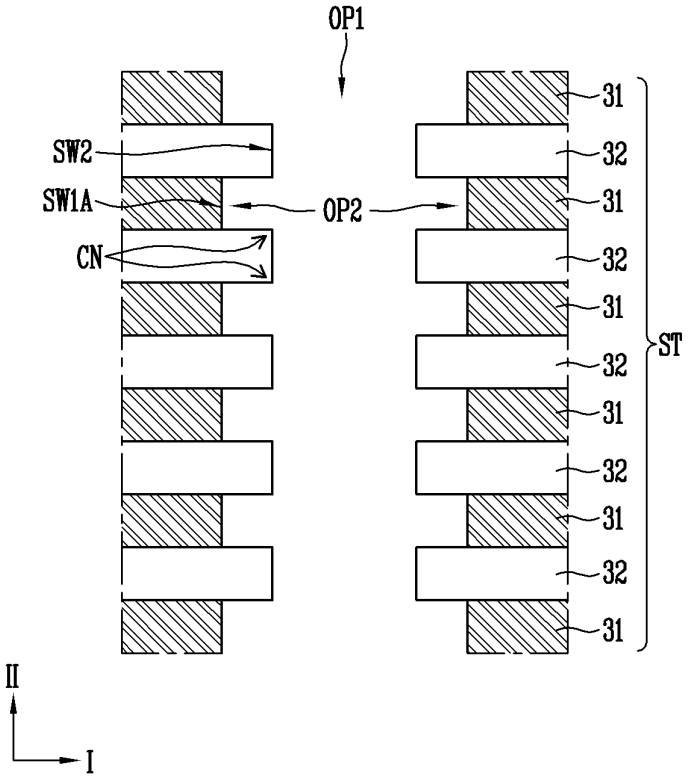


FIG. 3C

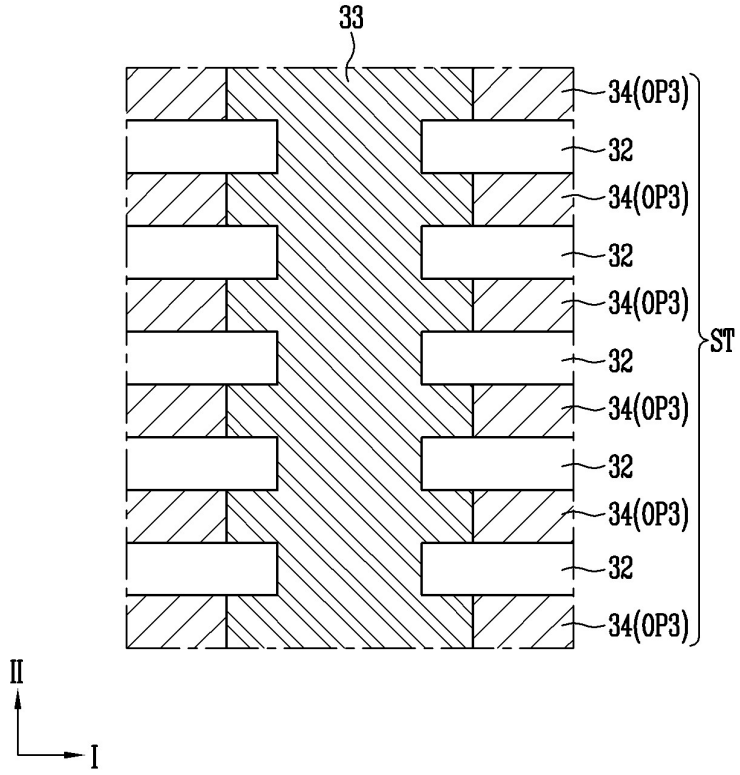


FIG. 3D

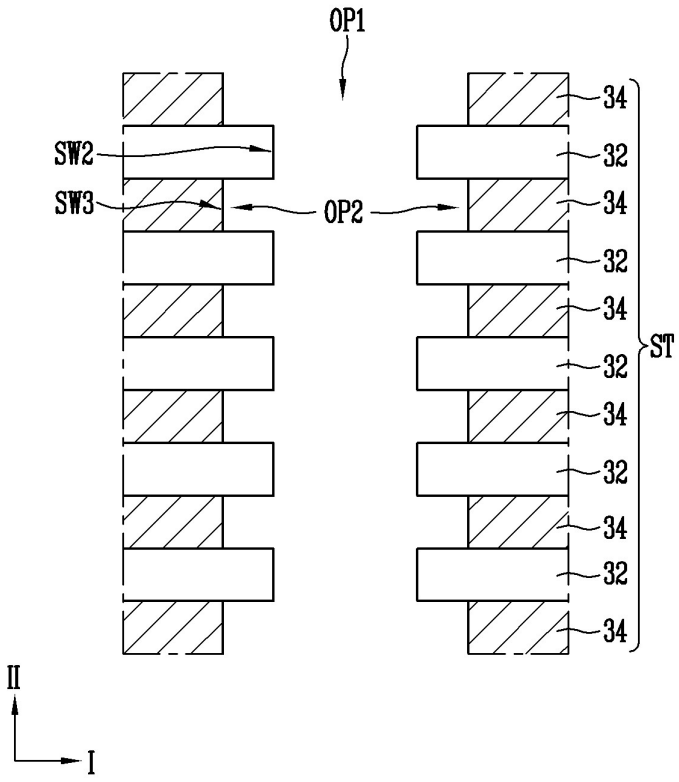


FIG. 3E

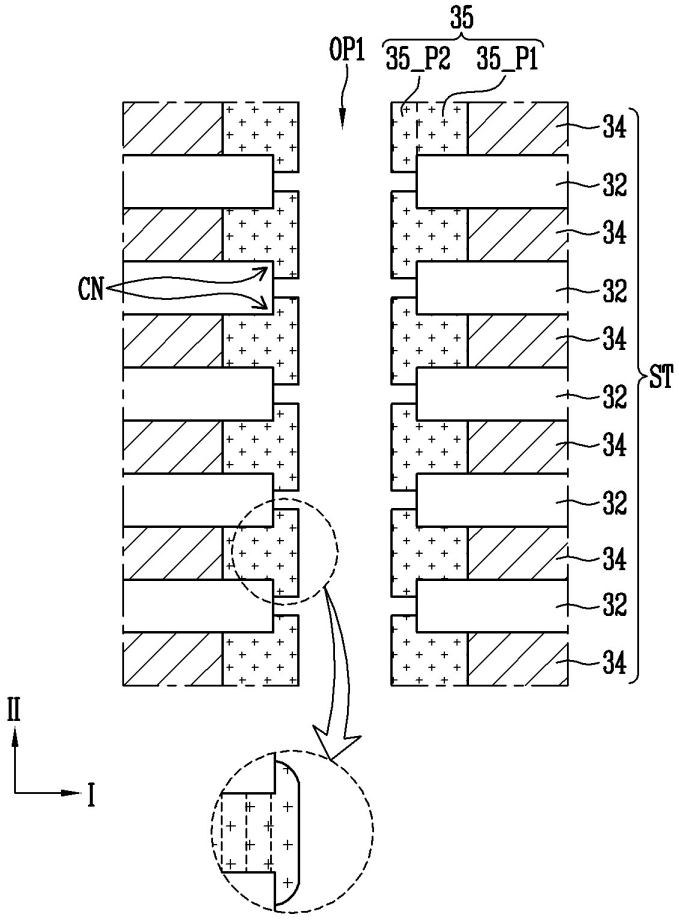


FIG. 3F

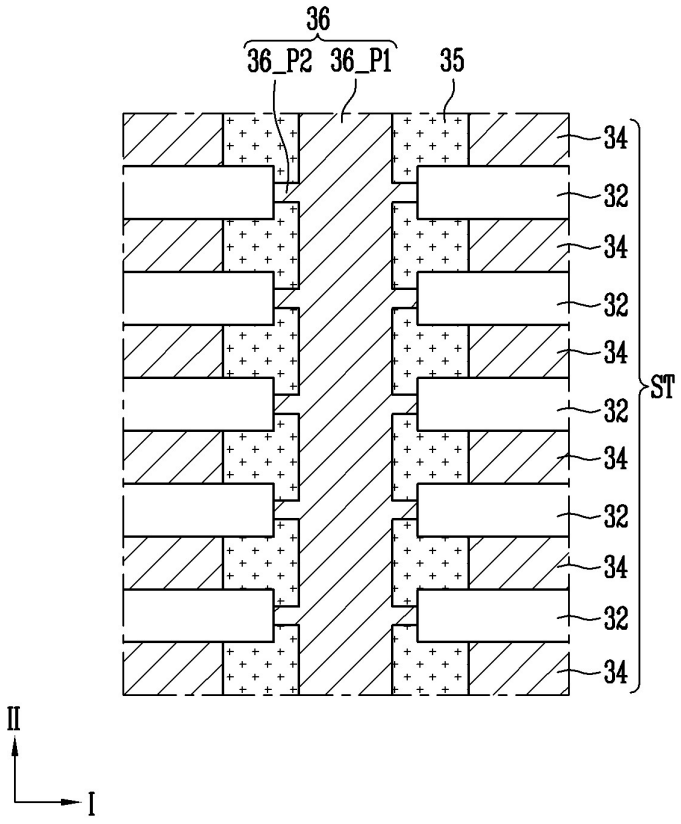


FIG. 4A

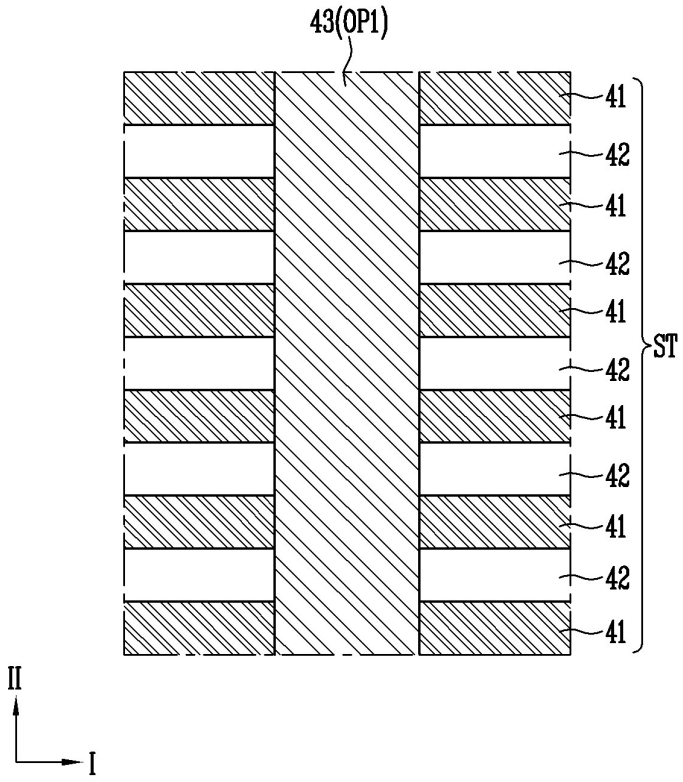


FIG. 4B

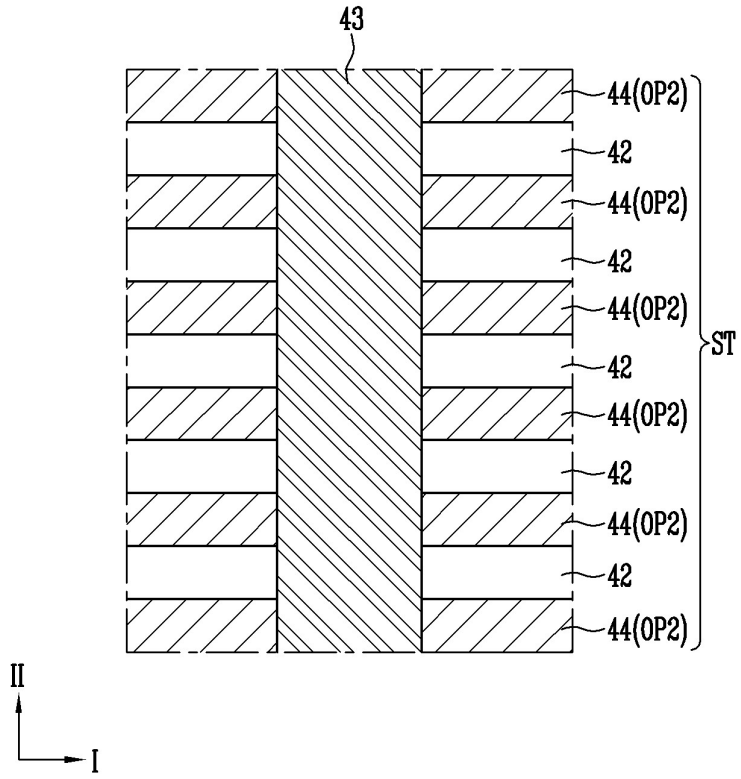


FIG. 4C

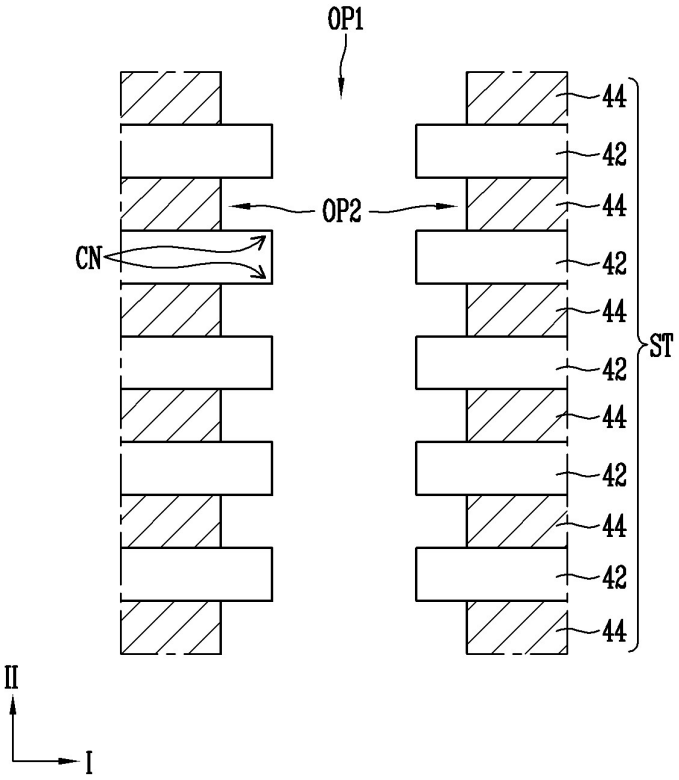


FIG. 4D

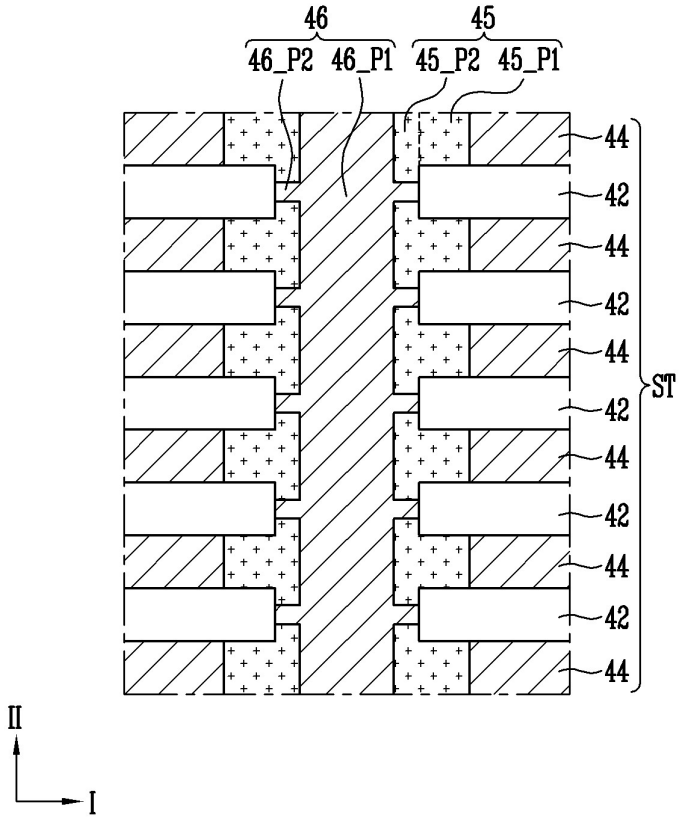


FIG. 5A

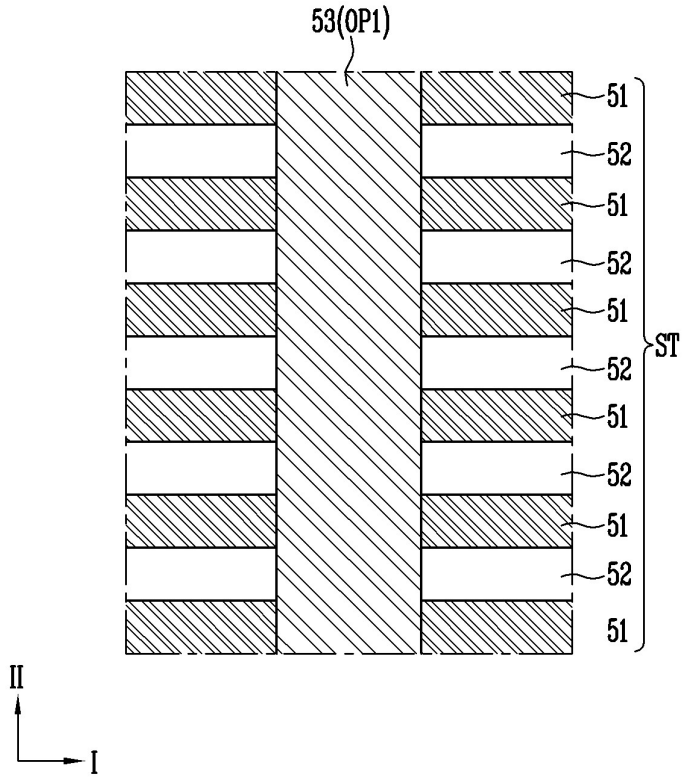


FIG. 5B

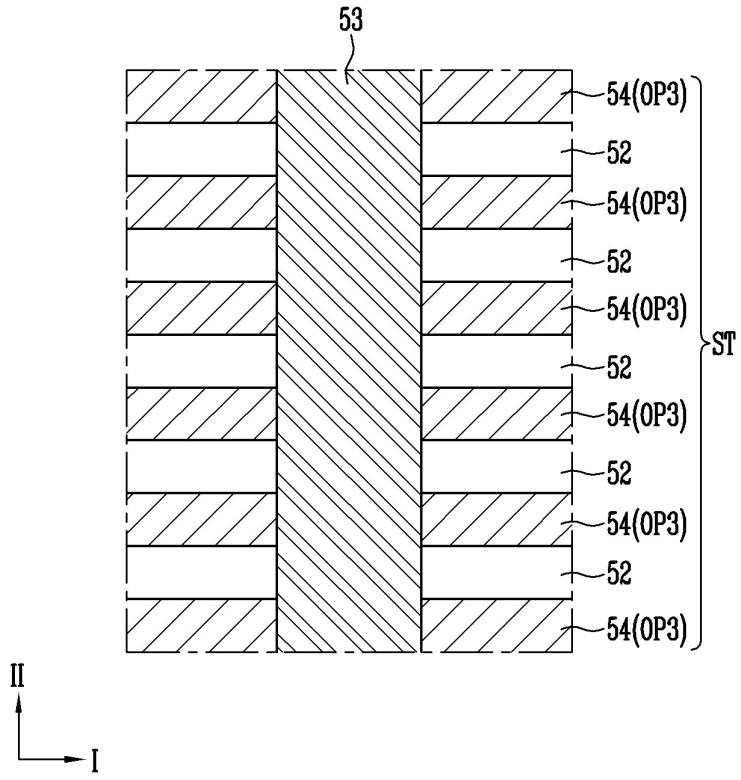


FIG. 5C

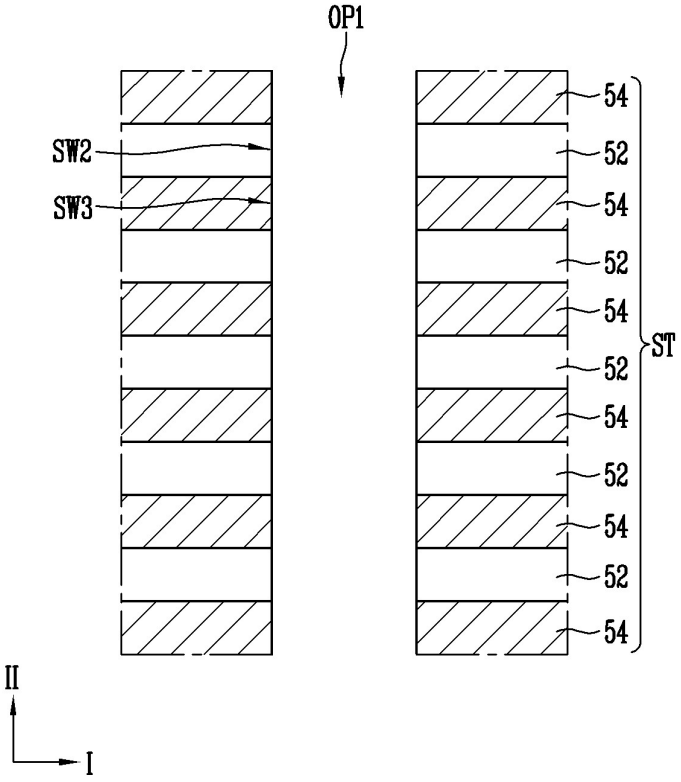


FIG. 5D

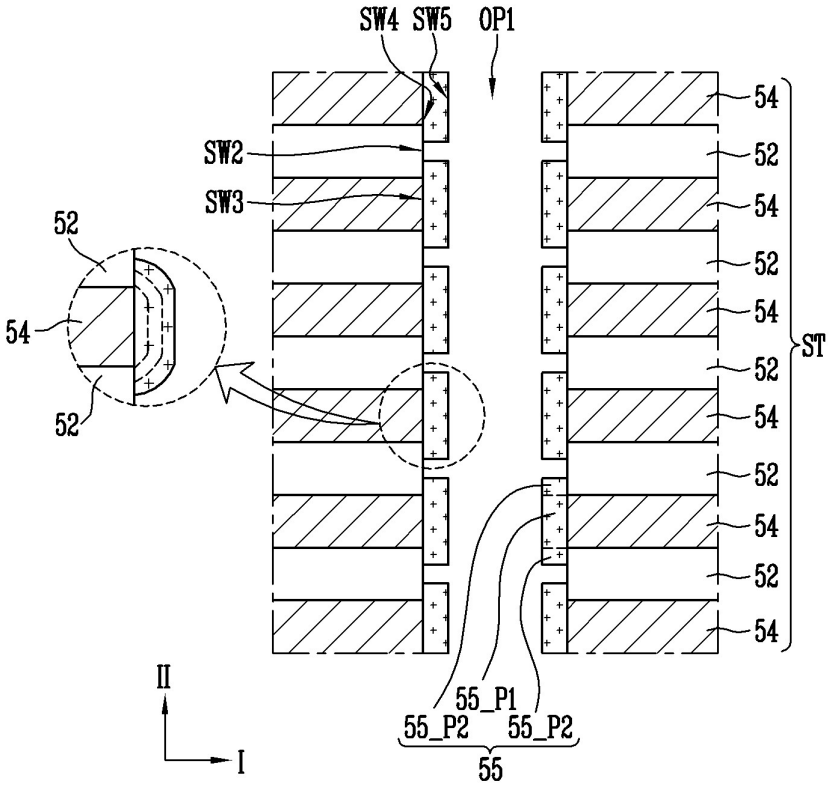

SW4
SW5
OP1
SW2
SW3
52
54
52
54
52
54
52
54
52
54
52
54
ST
II
I
55_P1
55_P2
55_P2
55

FIG. 5E

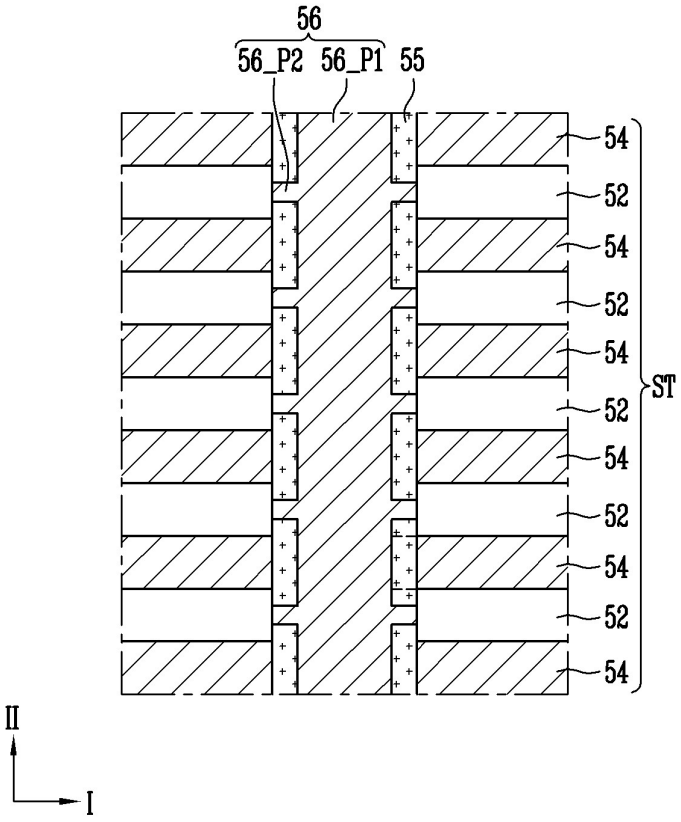


FIG. 6

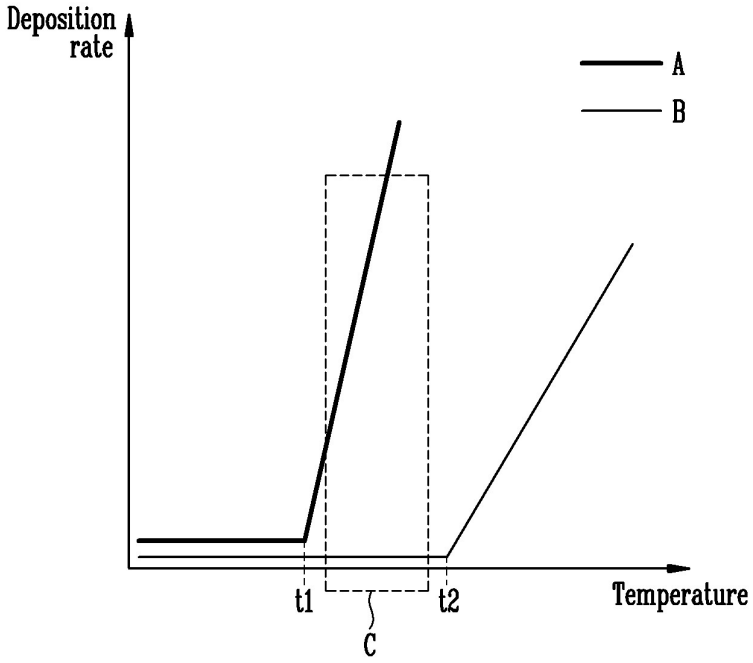


FIG. 7

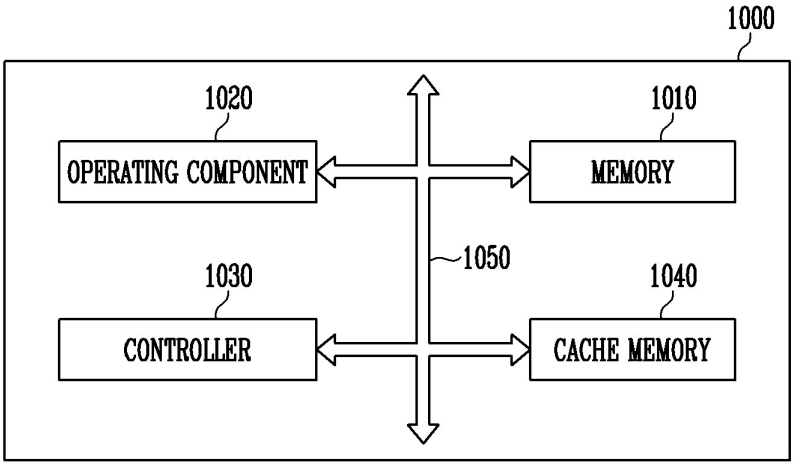

1000
1020
OPERATING COMPONENT
1010
MEMORY
1050
1030
CONTROLLER
1040
CACHE MEMORY

FIG. 8

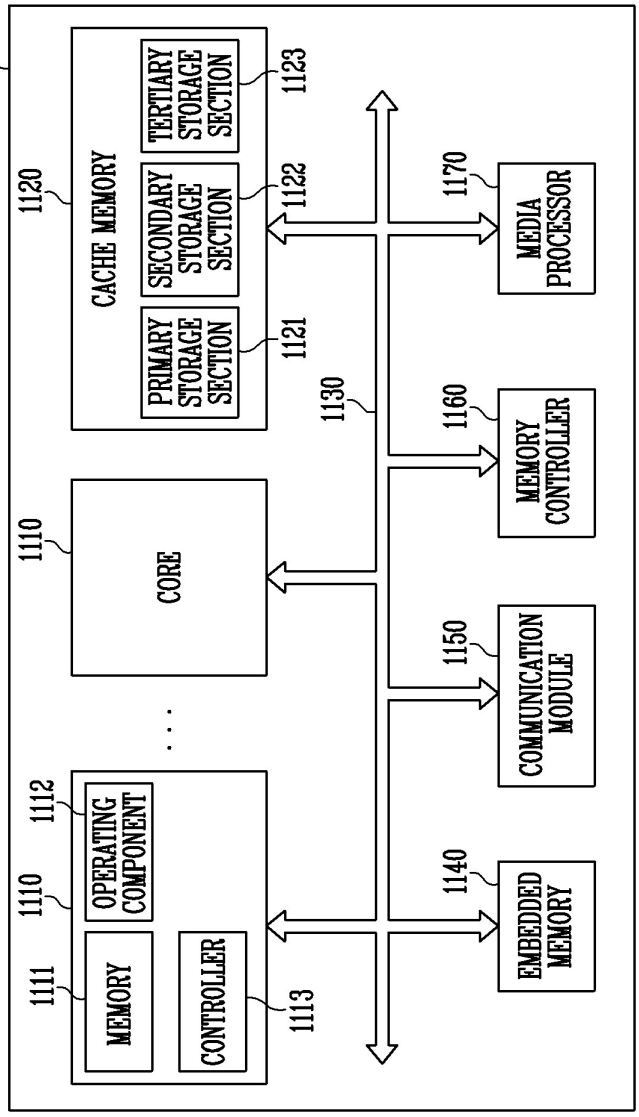

1100
CACHE MEMORY
1120
PRIMARY STORAGE SECTION
1121
SECONDARY STORAGE SECTION
1122
TERTIARY STORAGE SECTION
1123
CORE
1110
MEMORY
1111
OPERATING COMPONENT
1112
CONTROLLER
1113
1130
MEMORY CONTROLLER
1160
COMMUNICATION MODULE
1150
EMBEDDED MEMORY
1140
MEDIA PROCESSOR
1170

FIG. 9

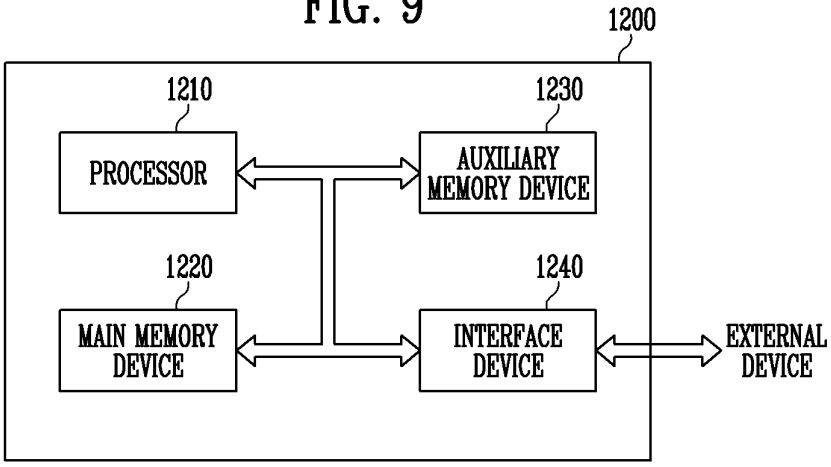
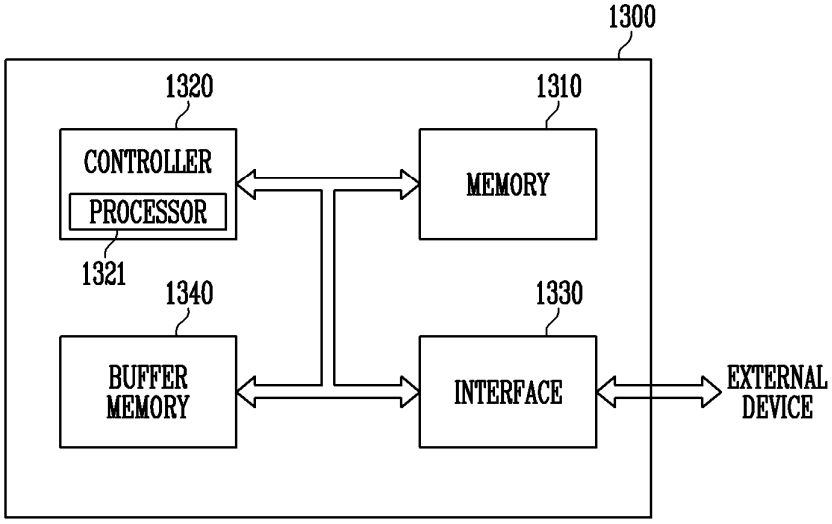

1200
1210
PROCESSOR
1230
AUXILIARY MEMORY DEVICE
1220
MAIN MEMORY DEVICE
1240
INTERFACE DEVICE
EXTERNAL DEVICE

FIG. 10


1300
1320
CONTROLLER
PROCESSOR
1321
1310
MEMORY
1340
BUFFER MEMORY
1330
INTERFACE
EXTERNAL DEVICE