



Description



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Methods for producing a semiconductor component and semiconductor component

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The invention relates to methods for producing a semiconductor component provided for mounting on a printed circuit board, the semiconductor component comprising a housing, which housing surrounds at least one semiconductor chip formed in planar fashion at least partially with a rear side area and/or side areas, the semiconductor chip being assigned electrical contacts by means of which an electrical connection to electrodes or electrode areas provided on the printed circuit board is to be produced, which electrical contacts are electrically connected to electrical contact areas on the front side of the semiconductor chip, which electrical contact areas are situated together within a significantly smaller contact-making region than the total area of the front side. The invention furthermore relates to a semiconductor component.

In large scale integrated and greatly miniaturized semiconductor components, the problem that occurs to an intensified extent after said components have been mounted on printed circuits (printed circuit boards) is that in the event of temperature fluctuations, on account of the different thermal expansion coefficients of the materials involved, strong mechanical stresses occur within the component and between the component and the printed circuit board. Figure 5 shows a customary design of such a miniaturized semiconductor module. The semiconductor component 1 is connected to the printed circuit board 2 by its electrical contacts 5. The semiconductor chip 3 in turn is connected to the interposer 12 by means of electrical contacts 14, the semiconductor chip being bonded to the interposer for

the purpose of mechanical stabilization by means of an underfiller 13. The semiconductor chip 3 is furthermore encapsulated with an encapsulation 15. The interposer 12 as carrier is often also completely encapsulated as well.

Owing to temperature fluctuations or variations, mechanical stresses occur in the known component forms on account of the different thermal expansion coefficients of the different materials. Figure 6 illustrates this in greater detail. The semiconductor chip 3 has a lower thermal expansion coefficient α than the interposer 12, which is produced from a different material. On account of the different expansion of the semiconductor chip and of the interposer, a strong mechanical stress 16 is transmitted via the underfiller 13, which is necessary for mechanical fixing and stabilization, and generated in the interposer 12. In order that a connection fracture of the electrical contacts 14 does not arise here, the thermal expansion coefficient of the interposer must already be adapted to the semiconductor chip. However, printed circuit boards 2 that are usually used have a thermal expansion coefficient that is greatly different from semiconductor chips. Therefore, the interposer 12, which is already under mechanical stress, exerts a strong mechanical stress 17 on the printed circuit board 2 via the electrical contacts 5 strained by said interposer. In the extreme case, this strong mechanical strain can lead to a deformation of the printed circuit board, which, particularly in the case of double-sided populations of printed circuit boards, may lead to the fracture of electrical contacts 5 and thus to the destruction of the electronic apparatus. If the deformation does not immediately lead to fracture in the choice of many instances of strain and strain relief it will then lead to fatigue of the material of the electrical contacts 5, which then again ultimately

leads to the fracture thereof and limits the service life. Moreover, the high degree of different expansion, and thus the mechanical strain, of the semiconductor component in itself, that is to say on the one hand
5 between semiconductor chip and interposer, and a semiconductor chip and encapsulation - in which a strain 18 is again induced - on the other hand, leads to fatigue of the electrical contacts 14, as a result of which the electrical contacts within the
10 semiconductor components 1 may also be destroyed.

Direct placement of a semiconductor chip onto a printed circuit board only by means of bumps, in order to prevent mechanical stresses or transmissions thereof
15 from interposed layers, does not achieve the goal either since a stable mechanical connection between the semiconductor chip and the printed circuit board cannot be produced by this means. Moreover, adhesive bonding of a chip by means of bumps with an underfiller, for
20 example in the form of a resist, would here only carry the direct strains from the semiconductor chip to the printed circuit board. This would again result in deformation of the printed circuit board, with the abovementioned difficulties. In particular, in the case
25 of printed circuit boards populated on both sides, it would lead to a destruction of circuits situated on one side of a printed circuit board or of the electrical contacts of said circuits.

30 In order that electronic circuits with a sufficiently long life can nevertheless be produced, complicated and thus expensive housing constructions are necessary for semiconductor components.

35 Therefore, it is an object of the invention to provide a method for producing a semiconductor component, and a semiconductor component in which the abovementioned

disadvantages do not occur and in which the very compact design is nevertheless made possible.

5 This object is achieved by means of the characterizing features of the production method of claim 1 and claim 11 and by means of a semiconductor component according to claim 39.

10 According to the invention, it is provided that a compliant buffer layer is applied on a rear plate, which at least forms the rear side area, that the semiconductor chip is thereupon applied to the compliant buffer layer by its rear side and fixed, that a compliant buffer layer is applied to and around the
15 semiconductor chip except for the region of the front side within which the contact areas are arranged, that a contact passage plate with a cutout provided over the contact areas is fixed on the compliant buffer layer on the front side of the semiconductor chip.

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The method according to the invention proposes that the semiconductor component be made in such a way that the very construction of the semiconductor component can preclude the arising of strains within the component or
25 with a printed circuit board on which the component is to be installed. As a result of the insertion of the buffer layer, the different thermal expansion coefficients of the different materials are compensated for and strains can no longer occur. This enables
30 adaptation to the thermomechanical properties of printed circuit board material, which enables a permanent, strain-free connection between printed circuit board (for example printed circuit) and semiconductor component. The components have a longer
35 life and the electronic circuits produced therewith can be used over a higher temperature range and can complete more hours of operation.

One refinement of the methods proposes that the side wall be produced in one piece together with the rear plate. Costly individual steps can be obviated as a result.

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Preferably, after the method step in which a compliant buffer layer is applied to and around the semiconductor chip at its front side and adjoining sides, a side wall forming the side areas of the housing is formed on the rear plate. Steps that are otherwise necessary necessary [sic] for the patterning of the side wall are obviated as a result.

15 An advantageous refinement of the methods provides for a plurality of semiconductor components to be produced simultaneously, the rear plates of the individual semiconductor components comprising a single mounting plate that is yet to be singulated to form individual rear plates in a later step. This enables the side walls to be produced in a particularly effective and inexpensive manner.

25 Following that, it is is [sic] advantageously provided that the boundary area is formed by a side of a compliant buffer layer of an adjacent semiconductor component. Additional auxiliary structures are avoided as a result.

30 A preferred refinement of the methods provides for the mounting plate to have the spatial extent and form of a wafer. This makes it possible to use existing production apparatuses and standardized sequences, which further reduces the costs of production.

35 In an advantageous manner, the buffer layer is also produced within the region of the electrical contact areas but only between the individual electrical contact areas on the front side of the semiconductor

chip. This reduces a temperature-dictated deformation of the opening relative to the surrounding structure.

5 The contact passage plate advantageously has material within its cutout but not over the electrical contact areas. This further reduces an undesirable deformation of the opening.

10 In accordance with a further method, it is provided that a stripping auxiliary layer is applied on a production carrier, that a spacer structure is applied on the stripping auxiliary layer, that a layer which forms a contact passage plate is applied on the stripping auxiliary layer around the spacing structure,
15 that a compliant buffer layer is applied on the layer forming the contact passage plate and around the spacer structure, that the semiconductor chip is fixed by its front side on the compliant buffer layer and on the spacer structure, the contact-making region being in
20 planar contact with the spacer structure, that the semiconductor chip is surrounded with a compliant buffer layer at its side areas and its rear side, that a rear plate, which forms at least the rear side area, is formed around the semiconductor chip and around the
25 compliant buffer layer.

What is proposed in this case, however, in contrast to the first method, is that an auxiliary carrier be used, which enables the spacer structure to be employed, as a
30 result of which the shaping and patterning of the recess around the region of the electrical contacts is configured in a simple and effective manner.

Preferably, after the method step in which a compliant
35 buffer layer is applied around the semiconductor chip, a side wall forming the side areas is formed on the production carrier.

In accordance with an advantageous method step, the side wall is formed on the production carrier by means of a casting process, material being cast into the interspaces between a boundary area and the compliant
5 buffer layer. This facilitates production and makes the latter inexpensive.

In accordance with a particularly preferred and advantageous method step, it is provided that a
10 plurality of semiconductor components are produced simultaneously, the boundary area being formed by a side of a compliant buffer layer of an adjacent semiconductor component on the production carrier. This enables particularly simple and sufficient mass
15 production without having to use additional structures or molds.

It is likewise advantageously provided that the rear plate and the side wall forming the side areas are
20 produced together, in particular in a casting or "molding" process. Work steps are additionally obviated as a result.

Preferably, the semiconductor component is separated
25 from the production carrier after the formation of the rear plate.

Following that, in accordance with a further method step, it is provided that after the separation from the
30 production carrier, an additional layer of a soft material is applied around the region of the electrical contact areas. This enables a softer transition between semiconductor chip and housing.

35 The stripping auxiliary layer and/or the spacer structure is advantageously chosen such that the latter can be removed by means of UV irradiation or a solution

which does not attack the semiconductor component. This ensures the stripping in a particularly simple manner.

5 Preferably, the spacer structure has an outer form essentially in the shape of a truncated cone or truncated pyramid. This ensures that no instances of contact with layers which are not desired take place.

10 An advantageous refinement of the method provides for the semiconductor chip to be fixed on the compliant buffer layer by being pressed into the latter and/or curing of the compliant buffer layer. That is particularly inexpensive and can be effected in one work operation with the placement, which makes further
15 adhesives or the like superfluous and obviates them.

Preferably, the buffer layer is produced between the housing and a side area of the semiconductor chip with a diameter G of at least

20
$$G := C \cdot \frac{\alpha_F - \alpha_C}{\alpha_G - \alpha_F}$$

where G is the diameter of the buffer layer between the housing and a side area of the semiconductor chip, C is the length of the solder from the side area to the central point of the semiconductor chip, α_C is the
25 thermal expansion coefficient of the semiconductor chip, α_G is the thermal expansion coefficient of the buffer layer and α_F is the thermal expansion coefficient of the housing.

30 In accordance with an advantageous refinement of the method, the electrical contacts are formed by bumps fixed to the semiconductor component.

Solder bumps are advantageously chosen as the bumps.
35 They can easily be fixed to the semiconductor component in one work operation.

Likewise in an advantageous manner, silicone bumps with electrical conducting areas led over them in a patterning or printing process for contact-making purposes or electrically conductive bumps essentially
5 composed of silicone ("compliant bumps") are chosen as the bumps.

The material of the buffer layer is preferably chosen such that the thermal expansion coefficient of the
10 buffer layer is greater than the thermal expansion coefficient of such printed circuit board material on which the semiconductor component is to be fixed. This compensates for the corresponding thermal expansion coefficient of the semiconductor chip, as a result of
15 which strains are effectively avoided.

Preferably, the material of the housing, in particular of the rear plate and/or contact passage plate and/or of the side wall, is chosen such that the thermal
20 expansion coefficient of the housing is equal to that of such printed circuit board material on which the semiconductor component is to be fixed. This avoids an undesired strain between housing and printed circuit board.

25 According to a further refinement, the material of the housing is chosen such that the thermal expansion coefficient of the housing is greater than that of the semiconductor chip.

30 A further advantageous refinement of the invention provides for the material of the buffer layer and of the semiconductor chip to be chosen such that the thermal expansion coefficient thereof together is equal
35 to that of the housing and/or to that of such printed circuit board material on which the semiconductor component is to be fixed.

Further advantages, special features and expedient developments of the invention emerge from the further subclaims or subcombinations thereof.

5 The invention is explained in more detail below with reference to the drawing, in which:

10 Figure 1 shows a semiconductor component according to the invention for mounting on a printed circuit board,

Figure 2 shows a detail view of the semiconductor component from figure 1,

15 Figure 3 shows a detail view from figure 1 in viewing direction III,

20 Figure 4 shows a diagram of the dimensioning of the elements of the semiconductor component,

Figure 5 shows a conventional semiconductor component mounted on a printed circuit board,

25 Figure 6 shows a diagrammatic illustration of strains of a conventional semiconductor component on a printed circuit board,

30 Figure 7 shows a diagrammatic method sequence according to a first production method in steps a to g from top to bottom,

Figure 8 shows a diagrammatic method sequence according to a variant in the production method in steps a to e from top to bottom,

35 Figure 9 shows a diagrammatic method sequence according to a second production method in steps a to g from top to bottom,

Figure 10 shows a diagrammatic method sequence for producing the electrical contacts in steps a to e from top to bottom, and

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Figure 11 shows an exemplary semiconductor component produced by the method.

In the figures, identical reference symbols designate identical or identically acting elements.

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Figure 1 diagrammatically shows a semiconductor component 1 according to the invention, which is provided for mounting on a printed circuit board. In this case, the semiconductor chip 3 is completely encapsulated by the housing 8 for protection from external effects. Within the housing 8, the semiconductor chip 3 is surrounded with a buffer layer 7 except for the product-making region 31. Within the contact-making region 31, the semiconductor chip 3 is connected via electrical contact areas 32 via line feeds 91 to the electrical contacts 5 in the form of bumps 6 (solder bumps 63), via which the electrical contact is made with the electrode areas provided for this purpose on the printed circuit board surface of the printed circuit board (not illustrated).

25

To the right of the central axis 34, the semiconductor component is provided with so-called compliant bumps 61, that is to say compliant bumps 6 as electrical contacts 5. In this case, the actual bumps 61 are formed by silicone shapings 62 which, in the example, for contact-making purposes, are coated with a thin, highly flexible metal strip 6a in order to enable the electrical contacts between bumps 6 and electrical contact areas 32.

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35

The semiconductor chip 3 is embedded softly in the elastic buffer layer 7, thus precluding a strain with the housing 8 and resultant deformation of the external dimensions of the semiconductor component 1.

5

Therefore, the different thermal expansion coefficients α of semiconductor chip and printed circuit board do not lead to strains since the different expansion between printed circuit board and semiconductor chip 3 is cushioned by means of the sufficiently compliant buffer layer 7. Moreover, the different expansion between semiconductor chip 3 and housing 8 no longer loads the inner contacts 32, 91, 5 since, by virtue of the central arrangement of the contacts in a narrow region of the total area of the chip, a temperature-dictated expansion with respect to the housing no longer leads to dislocations. Fatigue of the electrical contacts inside the semiconductor component and also on the outside of the semiconductor component is no longer brought about as a result of this. The service life is significantly increased.

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Figure 2 shows once again in more detailed fashion an exert from figure 1 with exerts serving for clarification, the dimensioning of the layer thicknesses being determined according to the according to the [sic] relationship

25

$$G := C \cdot \frac{\alpha_F - \alpha_C}{\alpha_G - \alpha_F}$$

where α_C is the thermal expansion coefficient of the semiconductor chip, α_G is the thermal expansion coefficient of the buffer layer 7, and α_F is the thermal expansion coefficient of the housing. C is the distance between the side area and the central axis 34. G represents the minimum value in this case.

35

Figure 3 shows a view in viewing direction III from figure 1. The contact-making region 31, within which

the electrical contact areas 32 are also situated, is significantly smaller than the mounting side area 33 and is situated in the center thereof.

5 Figure 4 shows, by way of example, a diagram in which the thickness G of the buffer layer 7 is plotted against half the semiconductor chip diameter C (in the example, central point of the chip on the central axis 34 to a side area 33, 35, 36). The gradient of 8.7%
10 results in this case from the assumed values for the thermal expansion coefficients as:

$$\begin{aligned}\alpha_c &= 3 \cdot 10^{-6} \text{ /K} \\ \alpha_g &= 300 \cdot 10^{-6} \text{ /K} \\ \alpha_F &= 16 \cdot 10^{-6} \text{ /K}\end{aligned}$$

15

The values in this case result for example as:

	y	x	z
Chip	5600	3000	470
Gap	504	270	42

where "Chip" denotes the values of the semiconductor chip 3 in its three spatial dimensions (x, y, z), and
20 "Gap" denotes the thickness G of the buffer layer 7 once again in its three spatial dimensions (x, y, z).

Figures 7a to 7g show in exemplary steps how the production method according to the first variant
25 proceeds.

Firstly, a compliant buffer layer 7 is applied on a mounting plate 41, which contains the rear plates 83 - which form the rear side areas 81 - in as yet
30 nonsingulated form.

The partial illustrations according to figures 7a to 7c here show variants of the patterning of compliant layers, which are intended to illustrate that it is not

absolutely necessary here to produce a continuous buffer layer 7.

Partial view 7d shows the semiconductor component 1
5 after mounting of the semiconductor chips 3, which are fixed on the compliant buffer layer 7 by their rear side 35.

Partial view 7e shows the state after application of
10 the buffer layer at the sides 36 and on the front side 33 of the chip 3, the contact-making region 31, within which the electrical contact areas 32 are located, not being covered in order to enable subsequent contact production with the electrical contacts.

15 The side walls 86 forming the side areas 82 have already been produced in partial view 7f; in this case, the interspaces 71 (see partial view 7e) between the individual sides 73 of the buffer layers 7 at the sides
20 36 of the semiconductor chips 3 - which in each case mutually form the boundary areas 72 - are potted with the material forming the side walls 86.

Partial view 7g shows the state after the fixing of the
25 contact passage plate 84 on the compliant buffer layer 7 on the front side 33 of the semiconductor chip 3. In this case, the contact passage plate 84 has a cutout 85 provided over the contact areas 32 [lacuna] that contact-making can still be effected. In this case, the
30 fixing can be effected by adhesive bonding or immediately directly by the formation of the contact passage plate 84 on the surface of the buffer layer 7.

A slight variation of the production method is shown in
35 exemplary individual steps in figures 8a to 8e. The difference with respect to the method shown in figures 7a to 7g is that, in accordance with partial view 8a, the side walls are produced first on the mounting plate

41. In this case, the side walls 86 may also have been produced at the same time as the mounting plate 41 in a casting process, for example, or, alternatively, be bonded thereon as finished grid.

5

The further sequence according to figures 8b to 8e is essentially identical to the sequence discussed in figures 7a to 7g, although this time rather than the buffer layers 7 forming the boundaries for the production process for the side walls, the situation is exactly the other way round.

Figures 9a to 9g show a production of semiconductor components according to the second variant of the production method.

Firstly, as illustrated in partial view 9a, a stripping auxiliary layer 43 is applied on a production carrier 42. A spacer structure 44 is applied on the stripping auxiliary layer 43. Said spacer structure serves for making a recess in the later housing wall.

As shown in partial view 9b, a layer which forms a contact passage plate 84 is applied on the stripping auxiliary layer 43 around the spacer structure 44.

Partial view 9c shows the state after a compliant buffer layer 7 has been applied on the layer forming the contact passage plates 84 and around the spacer structures 44.

The semiconductor chips 3 have already been fixed on the buffer layer 7 by their front side 3 in partial view 9d; in this case, the contact-making region 31 is in planar contact with the spacer structure 44 in order that this region is not covered later unnecessarily layers to be removed [sic].

Partial view 9e shows how the semiconductor chips 3 have been surrounded again with a compliant buffer layer 7 at their side areas 36 and their rear side 35. In this case, interspaces 71 are left in order to be
5 able to form the side walls 86 in the next step.

These side walls 86 have already been produced in partial view 9f, in a casting process with the rear plate 83 in the example shown.

10

Partial view 9g shows the state after the production carrier 42 has been stripped away and the as yet nonsingulated components have been freed of the stripping auxiliary layer 43 and the spacer structure
15 44. The production carrier may be stripped away for example by dissolving the - for example water-soluble - stripping auxiliary layer 43.

Figures 10a to 10e show the further contact-making
20 method for the semiconductor components 1, which are still unsingulated up that point according to production variants one and two.

Partial view 10a shows the initial situation of the
25 contact-making submethod with contact passage plates 84 that have been formed.

The formation of compliant bumps is shown below by way of example; it is equally possible here to form other
30 contact connections.

In accordance with partial view 10b, silicone bumps 62 are applied to the contact passage plates 84. These are then coated with metallic contact strips 91 running
35 away from the electrical contact areas 32 (partial view 10c). The metal strips may be fixed or produced by adhesive bonding, sputtering, a patterning process by means of lithography or a plating process or the like.

In partial view 10d, soldering resists 93 have been fixed to the undersides of the semiconductor components 1.

5

The separation of the individual finished semiconductor components 1 is effected by means of corresponding sawing cuts 92 in partial view 10e.

10 Figure 11 shows by way of example a variant of a semiconductor component 1 in which the housing section 86a has been widened for better distribution of the electrical contacts 5. It becomes clear that, however, the spatial dimensions remain the same in this case,
15 however, from buffer layer 7 to semiconductor chip 3.

List of reference symbols

	1	Semiconductor component
	2	Printed circuit board
5	3	Semiconductor chip
	31	Contact-making region
	32	Electrical contact area
	33	Mounting side area, front side
	34	Central axis
10	35	Rear side
	36	Sides of the semiconductor chip
	41	Mounting plate
	42	Production carrier
	43	Stripping auxiliary layer
15	44	Spacer structure
	5	Electrical contacts
	6	Bumps
	61	Compliant bumps
	62	Silicone bumps
20	63	Solder bumps
	6a	Metal strip
	7	Buffer layer
	71	Interspace
	72	Boundary area
25	73	Side of the buffer layer
	8	Housing
	81	Rear side area
	82	Side area
	83	Rear plate
30	84	Contact passage plate
	85	Cutout
	86	Side wall
	86a	Housing section
	91	Line beads
35	92	Storing cut
	93	Solder resist
	10	Surface of the printed circuit board
	12	Interposer

13	Underfiller
14	Electrical contacts
15	Encapsulation
16 to 18	Mechanical stress

Patent claims

1. Method for producing a semiconductor component (1)
provided for mounting on a printed circuit board,
5 the semiconductor component comprising a housing
(8), which housing (8) surrounds at least one
semiconductor chip (3) formed in planar fashion at
least partially with a rear side area (81) and/or
side areas (82), the semiconductor chip being
10 assigned electrical contacts (5) by means of which
an electrical connection to electrodes or
electrode areas provided on the printed circuit
board is to be produced, which electrical contacts
(5) are electrically connected to electrical
15 contact areas (32) on the front side (33) of the
semiconductor chip (3), which electrical contact
areas are situated together within a significantly
smaller contact-making region (31) than the total
area of the front side (33),
20 characterized
in that a compliant buffer layer (7) is applied on
a rear plate (83), which at least forms the rear
side area (81),
in that the semiconductor chip (3) is thereupon
25 applied to the compliant buffer layer (7) by its
rear side (35) and fixed,
in that a compliant buffer layer (7) is applied to
and around the semiconductor chip (3) except for
the region (31) of the front side (33) within
30 which the contact areas (32) are arranged,
in that a contact passage plate (84) with a cutout
(85) provided over the contact areas is fixed on
the compliant buffer layer (7) on the front side
(33) of the semiconductor chip (3).
35
2. Method for producing a semiconductor component,
according to claim 1,
characterized

in that a side wall (86) forming the side area (82) is produced in one piece together with the rear plate (83).

- 5 3. Method for producing a semiconductor component,
 according to claim 1,
 characterized
 in that, after the method step in which a
 compliant buffer layer (7) is applied to and
10 around the semiconductor chip at its front side
 (33) and adjoining sides (36), a side wall (86)
 forming the side areas (82) of the housing is
 formed on the rear plate (83).
- 15 4. Method for producing a semiconductor component,
 according to claim 3,
 characterized
 in that a prefabricated side wall (86) forming the
 side areas (82) is fixed on the rear plate (83) by
20 means of an adhesive bonding process or by means
 of a printing process.
5. Method for producing a semiconductor component,
 according to claim 3,
25 characterized
 in that the side wall (86) is formed on the rear
 plate (83) by means of a casting process, material
 being cast into the interspaces (71) between a
 boundary area (72) and the compliant buffer layer
30 (7).
6. Method for producing a semiconductor component,
 according to claim 5,
 characterized
35 in that a plurality of semiconductor components
 (1) are produced simultaneously, the rear plates
 (83) of the individual semiconductor components
 comprising a single mounting plate (41) that is

yet to be singulated to form individual rear plates (83) in a later step.

- 5 7. Method for producing a semiconductor component,
characterized
in that the boundary area (72) is formed by a side
(73) of a compliant buffer layer (7) of an
adjacent semiconductor component (1).
10
- 15 8. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the mounting plate (41) has the spatial
extent and form of a wafer.
- 20 9. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the buffer layer (7) is also produced
within the region (31) of the electrical contact
areas (31) but only between the individual
electrical contact areas on the front side (33) of
the semiconductor chip (3).
25
- 30 10. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the contact passage plate (84) has
material within its cutout (85) but not over the
electrical contact areas (32).
- 35 11. Method for producing a semiconductor component (1)
provided for mounting on a printed circuit board,
the semiconductor component comprising a housing
(8), which housing (8) surrounds at least one
semiconductor chip (3) formed in planar fashion at
least partially with a rear side area (81) and/or

side areas (82), the semiconductor chip (3) being assigned electrical contacts (5) by means of which an electrical connection to electrodes or electrode areas provided on the printed circuit board is to be produced, which electrical contacts (5) are electrically connected to electrical contact areas (32) on the front side (33) of the semiconductor chip (3), which electrical contact areas (32) are situated together within a significantly smaller contact-making region (31) than the total area of the front side (33), characterized

in that a stripping auxiliary layer (43) is applied on a production carrier (42), in that a spacer structure (44) is applied on the stripping auxiliary layer (43), in that a layer which forms a contact passage plate (84) is applied on the stripping auxiliary layer (43) around the spacing structure (44),

in that a compliant buffer layer (7) is applied on the layer forming the contact passage plate (84) and around the spacer structure (44),

in that the semiconductor chip (3) is fixed by its front side (33) on the compliant buffer layer (7) and on the spacer structure (44), the contact-making region (31) being in planar contact with the spacer structure (44), in that the semiconductor chip (3) is surrounded with a compliant buffer layer (7) at its side areas (36) and its rear side (35),

in that a rear plate (83), which forms at least the rear side area (81), is formed around the semiconductor chip (3) and around the compliant buffer layer (7).

35

12. Method for producing a semiconductor component according to claim 11, characterized

in that, after the method step in which a compliant buffer layer (7) is applied around the semiconductor chip (3), a side wall (86) forming the side areas (82) is formed on the production carrier (42).

5

13. Method for producing a semiconductor component according to claim 12, characterized

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in that the side wall (86) is fixed on the production carrier (42) by means of an adhesive bonding process or by means of a printing process.

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14. Method for producing a semiconductor component according to claim 12, characterized

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in that the side wall (86) is formed on the production carrier (42) by means of a casting process, material being cast into the interspaces (71) between a boundary area (72) and the compliant buffer layer (7).

25

15. Method for producing a semiconductor component according to claim 14, characterized

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in that a plurality of semiconductor components (1) are produced simultaneously, the boundary area (72) being formed by a side (73) of a compliant buffer layer (7) of an adjacent semiconductor component (1) on the production carrier (42).

35

16. Method for producing a semiconductor component according to one of claims 12, 14 or 15, characterized

in that the rear plate (83) and the side wall (86) forming the side areas (82) are produced together, in particular in a casting or "molding" process.

17. Method for producing a semiconductor component according to one of claims 11 to 16, characterized
in that the semiconductor component (1) is
5 separated from the production carrier (42) after the formation of the rear plate (83).
18. Method for producing a semiconductor component according to claim 17,
10 characterized
in that, after the separation from the production carrier (42), an additional layer of a soft material is applied around the region (31) of the electrical contact areas.
- 15 19. Method for producing a semiconductor component according to one of claims 11 to 18, characterized
in that the production carrier (42) has a spatial
20 extent and form like a wafer.
20. Method for producing a semiconductor component according to one of claims 11 to 19, characterized
25 in that the stripping auxiliary layer (43) and/or the spacer structure (44) is chosen such that the latter can be removed by means of UV irradiation or a solution which does not attack the semiconductor component (1).
- 30 21. Method for producing a semiconductor component according to one of claims 11 to 20, characterized
in that the spacer structure (44) has an outer
35 form essentially in the shape of a truncated cone or truncated pyramid.

22. Method for producing a semiconductor component according to one of claims 1 to 21, characterized
in that a plurality of semiconductor components
5 (1) are produced simultaneously and the individual semiconductor components that are produced together are separated from one another by means of a singulation process.
- 10 23. Method for producing a semiconductor component, according to one of claims 1 to 22, characterized
in that the semiconductor chip (3) is fixed on the compliant buffer layer (7) by being pressed into
15 the latter and/or curing of the compliant buffer layer.
24. Method for producing a semiconductor component, according to one of the preceding claims, characterized
20 in that the compliant buffer layer (7) is applied on the rear plate (83) and/or the contact passage plate (84) and/or around and on the semiconductor chip (7) by means of a printing process.
- 25 25. Method for producing a semiconductor component, according to one of the preceding claims, characterized
in that the cutout (85) in the contact passage
30 plate (84) is larger than the opening on the compliant buffer layer (7) around the electrical contact areas (32).
26. Method for producing a semiconductor component,
35 according to one of the preceding claims, characterized
in that a polymer plastic, ceramic, glass, epoxy resin or metal is chosen as material of the

contact passage plate (84) and/or of the rear plate (83) and/or of the side wall (86).

27. Method for producing a semiconductor component,
5 according to one of the preceding claims,
characterized
in that the buffer layer (7) is produced between
the housing (8; 82, 83, 84) and a side area (33,
35, 36) of the semiconductor chip (3) with a
10 diameter G of at least

$$G := C \cdot \frac{\alpha_F - \alpha_C}{\alpha_G - \alpha_F}$$

- where G is the diameter of the buffer layer (7)
between the housing (8) and a side area (33, 35,
36) of the semiconductor chip (3), C is the length
15 of the solder from the side area to the central
point of the semiconductor chip (3), α_C is the
thermal expansion coefficient of the semiconductor
chip (3), α_G is the thermal expansion coefficient
of the buffer layer (7) and α_F is the thermal
20 expansion coefficient of the housing (8).

28. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
25 in that the electrical contacts (5) are formed by
bumps (6) fixed to the semiconductor component
(1).

29. Method for producing a semiconductor component,
30 according to one of the preceding claims,
characterized
in that solder bumps are chosen as the bumps (6).

30. Method for producing a semiconductor component,
35 according to one of the preceding claims,
characterized

in that silicone bumps (62) with electrical
conducting areas (6a) led over them in a
patterning or printing process for contact-making
purposes or electrically conductive bumps
essentially composed of silicone ("compliant
bumps") are chosen as the bumps (6).

31. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the semiconductor component (1) is
produced in a WLP ("wafer level package") flip-
chip or CSP design ("chip scale package").
32. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the material of the buffer layer (7) is
chosen such that the thermal expansion coefficient
of the buffer layer is greater than the thermal
expansion coefficient of such printed circuit
board material on which the semiconductor
component (1) is to be fixed.
33. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the buffer layer (7) is highly elastic
and/or thermally conductive.
34. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
in that the material of the housing (8), in
particular of the rear plate (83) and/or contact
passage plate (84) and/or of the side wall (86),
is chosen such that the thermal expansion
coefficient of the housing is equal to that of

such printed circuit board material on which the semiconductor component (1) is to be fixed.

35. Method for producing a semiconductor component,
5 according to one of the preceding claims,
characterized
in that the material of the housing (8) is chosen
such that the thermal expansion coefficient of the
housing is greater than that of the semiconductor
10 chip (3).
36. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
15 in that the material of the buffer layer (7) and
of the semiconductor chip (3) is chosen such that
the thermal expansion coefficient thereof together
is equal to that of the housing (8) and/or to that
of such printed circuit board material on which
20 the semiconductor component (1) is to be fixed.
37. Method for producing a semiconductor component,
according to one of the preceding claims,
characterized
25 in that the buffer layer (7) is composed of a
polymer, in particular silicone or polyurethane.
38. Method for producing a semiconductor component,
according to claim 37,
30 characterized
in that the buffer layer (7) is composed of a
foamed material.
39. Semiconductor component,
35 characterized
in that it is produced by a method according to
one of claims 1 to 38.