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AN EFFICIENT SEMICONDUCTOR BURN-IN CIRCUIT AND METHOD OF OPERATION

ABSTRACT

The disclosed invention provides a circuit and burn-in test method for semiconductor devices (12) that increases the speed of burn-in tests. The present invention accomplished this by causing each of the devices (12) under test to be tested multiple times (from 2 to 32+ times) during each power cycle. By such multiple cycling of the unit (12) under test, during the power cycle, the total test time is shortened. It has also been found that the devices (12) tested, in accordance with the present invention are more efficiently stressed and have a reliability greater than devices (12) passing the prior art tests.

Fig. 3



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