Memory Management

The invention relates to memory devices, and, in particular, to memory management of devices for computer systems and the like. It finds particular application in memory systems that use partially working memory circuits where defective rows, columns, bits or bytes in the main memory circuit are replaced by good rows, columns, bits or bytes from a supplementary store (usually called a substitute store). These memory systems may include the controlling means to disable a defective area when it is being accessed and enable a replacement area. This controlling means is referred to as a partial memory engine.

In the semiconductor industry, solid state memory devices are fabricated as dice on wafers of silicon, each die containing a memory array. These dice are tested and those which can be made to work perfectly are packaged for use. The other dice, those which contain one or more defective memory cells, are usually either discarded or used in some fault tolerant memory device.

Our co-pending international patent application PCT/GB94/00577 relates to the control of memory systems using a partial memory engine. We have now devised a more flexible arrangement for replacing bits, bytes, rows or columns in which some of the circuitry can be configured in a number of different ways.

The invention will now be particularly described, by way of example, with reference to the accompanying drawings, in which

Figure 1 shows a diagram of blocks in a RAM (random access memory) chip which has faults in part of the rows and columns;

Figure 2 shows a pictorial representation of part of a fault tolerant memory;

Figure 3 shows a diagram of part of a fault tolerant memory; and

Figure 4 shows a diagram of one slice from a fault tolerant memory.

Some memory circuits, for example DRAMs (Dynamic Random Access Memories) are composed of a number of planes (typically four, eight, or sixteen), with each plane containing a number of blocks of memory cells. Figure 1 illustrates the case where one plane is composed of sixteen blocks, although in this type of arrangement all four rows in a block usually share the same row address and all four columns in a block usually share the same column address. It is common in memory circuits to have block failures within

a row or a column. Thus it would be desirable to be able to detect when a defective block within a row or column is being accessed and to substitute a block for that block.

In Figure 1 the four columns are labelled MSB 11, MSB 10, MSB 01, and MSB 00. The reason for this type of labelling is that rows in the blocks are usually selected by the most significant bits of the column address. Where there are four columns of blocks then the two most significant bits are used, where there are eight columns of blocks then the three most significant bits are used (since $2^3 = 8$), and so on. In the example of Figure 1 the two most significant bits from the column address are required to locate the block of columns and the full row address is required to locate the defective row.

In Figure 2 there are a number of blocks, representing the function of a fault tolerant memory made according to the present invention. When an entire row from a block in a plane is being substituted then the full row address 2 is decoded together with the N most significant bits of the column address, where N = log2 (the number of blocks in a column). The remaining bits in the column address (the least significant bits) 4 are decoded to address the memory cells 6. The output of the memory cells 6 is sent to a router 8 accompanied by data routing information 10 which informs the router of which data bits need to be replaced by the bits from the memory cells 6.

In Figure 3 there are a number of slices 12. Each slice 12 (as shown in more detail in Figure 4) includes a register 14 to contain the address of a faulty memory location, a comparator 16 to compare the incoming address 18 with the address stored in the register 14, substitute memory cells 6 to replace defective bits from a main memory, a bit select register 20 to hold the substitute bits, a bit relocation register 22 to determine which particular bit (or bits) needs to be substituted, and a data bus 24 on which the substitute data is placed. The bit relocation register is essential because it ensures that the correct bit is replaced from the main memory. An address decoder 26 is used to decode a portion of the row or column address which is used to address main memory. There are also two registers 28 and 30 for holding the relevant portion of the row or column address.

One aspect of the present invention is the use of only a portion of the incoming address in the comparator circuitry. The incoming address is in the form of x bits for the row address and y bits for the column address, where x is typically twelve and y is typically twelve, although the invention is not restricted to these or similar numbers of address bits.

In other embodiments, individual bits may be replaced by means of the partial memory engine. Since most faulty memory circuits contain relatively few errors (compared with the total number of memory cells) it is unlikely in most cases that there will be other defective bits in the same row or column with the same bit sequence of three or four bits in the least significant portion of the address.

In a further embodiment, a memory system has the following characteristics. There is a ten bit row address, a ten bit column address, sixteen blocks in each plane (two rows of eight blocks) and a faulty row in one of the blocks. In this situation all ten bits in the row would be compared with the incoming row address but only the three most significant bits of the incoming column address would be compared with the corresponding three bits from the stored column address. The other (or at least some of the other) bits of the column address would be used to address the memory cells.

Provided there are not two defective bits in the row selected by the full address with errors at column addresses containing the same bit sequence over the three chosen bits, then the abbreviated column address will still uniquely access the defective location. It should be noted that if a row has more than one fault then the bits from the column address chosen for comparison must be different for all of the faults, otherwise the bit sequence would not uniquely address each fault.

The present arrangement is very flexible because the bits chosen for each defective location can be different for each slice. If there were a column error in one of the blocks then it would be preferable to use the full column address and a curtailed row address rather than the full row address and a curtailed column address. With certain embodiments both of these options (full row - partial column, and partial row - full column) may advantageously be used. It should be emphasised that each slice is separately configurable. This means that one slice might compare the full row address and the three least significant bits of the column address, the next slice might compare the full column address and the three least significant bits of the row address. It is not essential to the operation of the invention that three bits are used. In some embodiments more bits might be used, in others fewer bits might be used.

The configuration of the memory cells will depend on the type of replacement policy that is being implemented by the partial memory engine. In one of the above

examples it was a block row or column replacement policy that was being implemented. Therefore, the memory cells used in the above embodiment would only have to be addressable in individual blocks. i.e. they would not have to be bit addressable. However, if a bit replacement system were being used in conjunction with a 1k by 1 memory, then the memory would have to be addressed by ten address bits (since $2^{10} = 1k$) so that each location could be uniquely addressed. The ten bits would come from the least significant bits of either the row or column address, whichever was not being used as an input to the comparator. The least significant address bits are used to ensure that there is a continuous range of addresses. This is essential to be able to address each location in the memory cell array.

It will be appreciated that various modifications may be made to the above described embodiments within the scope of the present invention.

CLAIMS

1. Memory management apparatus including means for replacing a defective storage locations with a functional storage location comprising receiving means for receiving an address for accessing said storage location, comparing means for comparing the address for accessing a storage location with addresses of known defective storage locations, and directing means for directing accesses to an alternative location when the address for accessing a storage location matches one of the addresses of known defective storage locations **characterised in that** said comparator means is adapted to decode only a portion of the address for accessing said storage location

2. Memory management apparatus according to claim 1, **characterised in that** the receiving means are adapted to receive an address as a row and column address.

3. Memory management apparatus according to claim 1 or claim 2 **characterised in that** said comparator means is adapted to use a full row address and a partial column address.

4. Memory management apparatus according to claim 1 or claim 2 **characterised in that** said comparator means is adapted to use a full column address and a partial row address.

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