

ABSTRACT

A semiconductor device includes first, second, and third bitlines in a memory cell array region and an extension region. Each of the first, second, and third bitlines includes a line portion, a connection portion, a pad portion, and an extension portion. The line portions of the first and second bitlines are in the memory cell array region and the extension region. The connection portions, the pad portions, and the extension portions of the first and second bitlines are in the extension region. An end portion of the line portion of the third bitline is between the extension portions of the first and second bitlines. Widths of the extension portions of the first and second bitlines decrease from the pad portions of the first and second bitlines. The end portion of the line portion of the third bitline has a convex shape.

FIG. 1