CLAIMS

I/We claim:

1. A method for fabricating a semiconductor device, comprising:

forming a first metallization layer and a second metallization layer on a semiconductor substrate, the second metallization layer being in electrical contact with the first metallization layer by a first via in a dielectric layer vertically spaced apart the first metallization layer and the second metallization layer;

forming an interconnect aperture at least partially in the semiconductor substrate after the first metallization layer is formed;

forming an aperture insulator portion on a top surface of the second metallization layer, the aperture portion insulator having a first lateral dimension smaller than a second lateral dimension of the second metallization layer, the aperture insulator portion being formed at a location that laterally divides the second metallization layer into a contact portion and a non-contact portion, the contact portion being substantively smaller than the non-contact portion, the contact portion and the non-contact portion being defined by a side of the aperture insulator portion; and

filling the interconnect aperture with a conductive material to form a conductive interconnect extending at least partially through the semiconductor substrate, wherein the conductive interconnect includes a vertical section in the interconnect aperture and a horizontal section external to the interconnect aperture, and wherein the horizontal section includes a substantially-planar bottom surface, and wherein the horizontal section extends laterally toward the second metallization layer such that a portion of the substantially-planar bottom surface of the horizontal section is in physical contact with the top surface of the contact portion of the second metallization layer at a first horizontal location, and wherein the non-contact portion is electrically coupled to the first metallization layer at a second horizontal location different from the first horizontal location, and wherein the second metallization layer is in electrical contact with the conductive interconnect, and wherein the side of the aperture insulator portion faces the vertical section of the conductive interconnect, and wherein the first via is

vertically aligned with the non-contact portion, and wherein the contact portion of the second metallization layer extends vertically from an upper surface of the dielectric layer to a lower surface of the horizontal section of the conductive interconnect.

2. The method of claim 1 wherein:

the conductive material is a first conductive material; and

forming an interconnect aperture includes:

depositing a dielectric on the second metallization layer;

forming the interconnect aperture through the dielectric and the semiconductor substrate;

exposing at least a portion of the second metallization layer; and

depositing a second conductive material in the interconnect aperture and onto the exposed portion of the second conductive material.

3. A method for fabricating a semiconductor device, comprising:

forming a plurality of metallization layers carried by a semiconductor substrate, the plurality of metallization layers including at least a first metallization layer and a second metallization layer, wherein the second metallization layer is spaced apart from the semiconductor substrate with the first metallization layer therebetween, the second metallization layer being in electrical contact with the first metallization layer by a first via in a dielectric layer vertically spaced apart the first metallization layer and the second metallization layer;

forming an interconnect aperture at least partially in the semiconductor substrate;

forming an aperture insulator portion on a top surface of the second metallization layer, the aperture insulator portion being laterally smaller than the second metallization layer, the aperture insulator portion being formed at a location that laterally divides the second metallization layer into a contact portion and a non-contact portion, the contact portion being substantively smaller than the non-contact portion, the contact portion and the non-contact portion being defined by a side of the aperture insulator portion;

forming a conductive interconnect extending at least partially through the semiconductor substrate, wherein the conductive interconnect includes a vertical section in the interconnect aperture and a horizontal section external to the interconnect aperture, and wherein the horizontal section includes a substantially-planar bottom surface, and wherein the horizontal section extends laterally toward the second metallization layer such that at least a portion of the substantially-planar bottom surface of the horizontal section is in physical contact with the top surface of the contact portion of the second metallization layer at a first horizontal location, and wherein the non-contact portion is electrically coupled to the first metallization layer at a second horizontal location different from the first horizontal location, and wherein the side of the aperture insulator portion faces the vertical section of the conductive interconnect, and wherein the conductive interconnect is in electrical contact with the second metallization layer, and wherein the first via is vertically aligned with the non-contact portion, and wherein the contact portion of the second metallization layer extends vertically from an upper surface of the dielectric layer to a lower surface of the horizontal section of the conductive interconnect.

4. The method of claim 3 wherein forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the first metallization layer is formed.

5. The method of claim 3 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the second metallization layer is formed;

the method further includes exposing at least a portion of the second metallization layer; and

the conductive interconnect is formed by filling the interconnect aperture with a conductive material;

filling the interconnect aperture includes introducing the interconnect material into the interconnect aperture and onto the exposed portion of the second metallization layer.

6. The method of claim 1 wherein:

the conductive material in the interconnect aperture includes a first end and a second end opposite the first end;

the second metallization layer includes a first portion generally corresponding to the conductive material in the interconnect aperture and a second portion extending laterally from the first portion; and

the first end of the conductive material in the interconnect aperture is electrically coupled to the first portion of the second metallization layer

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7. The method of claim 3 wherein:

the conductive material in the interconnect aperture includes a first end and a second end opposite the first end;

the second metallization layer includes a first portion generally corresponding to the conductive material in the interconnect aperture and a second portion extending laterally from the first portion; and

the first end of the conductive material in the interconnect aperture is electrically coupled to the first portion of the second metallization layer

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8. The method of claim 1, further comprising:

forming an insulation between the semiconductor substrate and the first metallization layer;

positioning an integrated circuit on or in the semiconductor substrate;

forming a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer; and

forming a dielectric between the first and second metallization layers, wherein the dielectric includes a conductive via directly between the first metallization layer and the second metallization layer

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9. The method of claim 1, further comprising:

forming a third metallization layer spaced apart from the semiconductor substrate by the first and second metallization layers.

10. The method of claim 1, wherein the vertical section and the horizontal section are made of a common material.

11. The method of claim 3, further comprising:

forming an insulation between the semiconductor substrate and the first metallization layer;

positioning an integrated circuit on or in the semiconductor substrate;

forming a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer; and

forming a dielectric between the first and second metallization layers, wherein the dielectric includes a conductive via directly between the first metallization layer and the second metallization layer.

12. The method of claim 3, further comprising:

forming a third metallization layer spaced apart from the semiconductor substrate by the first and second metallization layers.

13. The method of claim 3, wherein the vertical section and the horizontal section are made of a common material.

14. The method of claim 1, further comprising:

forming a dielectric layer on the top surface of the second metallization layer.

15. The method of claim 14, wherein the dielectric layer is made of a first material, and wherein the aperture insulator portion is made of a second material different than the first material.

16. The method of claim 3, further comprising:
forming a dielectric layer on the top surface of the second metallization layer.

17. The method of claim 16, wherein the dielectric layer is made of a first material, and wherein the aperture insulator portion is made of a second material different than the first material.