

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO MONOLITHIC
 INTEGRATED CIRCUIT STRUCTURES AND TO
 ELECTRONIC TIMEPIECES INCORPORATING THE SAME

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company, of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to monolithic integrated circuit structures and to electronic timepieces incorporating the same.

The main object of the invention is to provide improved monolithic integrated circuit structures which lend themselves well to miniaturisation and can be constructed on a very small chip; which shall be economic to manufacture; which shall be of relatively low electric power consumption; and which shall be at the same time such as to embody circuit portions requiring operating power voltages of different values. Although not limited exclusively thereto, the invention is most advantageous for and is primarily intended for, use in the circuitry of electronic timepieces. When used for this application the invention facilitates the provision of an electronic timepiece of relatively small size and cost and relatively low power consumption and which is such that different operating voltages are used for the normally provided time-standard oscillator and frequency divider of the timepiece (on the one hand) and for the display driving circuit thereof (on the other hand).

Of recent years the power consumption of the electronic circuits of an electronic timepiece has been considerably reduced by making use of complementary metal oxide semiconductor (C-MOS) circuits in the timepiece. However C-MOS circuits are still of relatively high power consumption when used at relatively high frequencies such as are normally employed for the time standard oscillator of a timepiece and in at least the high frequency portions of the frequency divider normally provided to divide the frequency of the oscillator to a relatively low frequency suitable for the display driving circuit of the

timepiece. It is therefore highly desirable that the operating supply voltage for these parts of the timepiece circuitry shall be as low as possible. A fairly modern development in electronic watches and other timepieces is the replacement of the conventional, mechanically driven display using hands for displaying time, by purely electrical displays using a liquid crystal or a light emitting diode type of digital display of time. Displays of these types, however, require relatively high operating voltage supplies. In a timepiece having a time standard oscillator, a frequency divider, a display driving circuit and a display of the liquid crystal type or of the light emitting diode type, there are substantial practical advantages to be gained by using a lower supply voltage for the oscillator and the divider than for the driving circuit.

In timepieces using monolithic integrated circuits for the circuitry thereof, and with monolithic power sources, there may be serious defects if the same operating voltage is used both for the display driving circuit and for the time standard oscillator and the frequency divider. In a timepiece with a liquid crystal type of display a relatively high voltage—usually of somewhere between 3 and 6 volts—is required for the driving circuit for the display and if the same voltage is used for the oscillator and for the frequency divider, these parts of the integrated circuit structure must have an undesirably high breakdown voltage and this of course involves the provision of a chip of a larger size than would otherwise be possible as well as a larger power consumption. If the timepiece has a display of the light emitting diode type, a relatively low voltage can be used for the driving circuit (e.g. 1 to 5 volts) but if such a voltage is used a relatively large current is required in order to provide a reliable drive to the display and the circuit portion used as the driving circuit must be made relatively large because of this current at low voltage.

The present invention seeks to overcome these defects.

According to this invention, there is provided an electronic circuit structure composed of complementary MOS transistors, and comprising a circuit portion requiring a relatively high operating supply voltage and a circuit portion requiring a relatively low operating supply voltage, wherein said circuit portions are of monolithic integrated circuit construction and are connected, one to the other, through a signal interface which adapts the logic levels of said portions are adapted to one another.

The structure may comprise C-MOS elements constituting P-channel and N-channel transistors, the former being formed on an N-type substrate and the latter being formed by P-type islands on said substrate. In one embodiment of this nature P-type areas are formed on the substrate and N-type diffusions are formed therein to provide transistor drains and sources, the drains of each pair of those transistors which are adjacent to one another being respectively coupled so as to be common to each other and metal electrodes are provided to constitute gates for the transistors, the arrangement being such that each transistor source is connected with the substrate on which it is formed.

An electronic timepiece in accordance with the invention includes, in the circuitry thereof, an electronic circuit structure as above defined. In such a timepiece that circuit portion of the integrated circuit structure which requires the relatively high voltage may be employed for the driving circuit for driving the time display of the timepiece and circuit portions of the integrated circuit structure requiring the relatively low voltage may be employed for the time standard oscillator of the timepiece and for a frequency divider provided therein for dividing the oscillator frequency down to a relatively low frequency for the time display driving circuit of the timepiece. The input frequency to the time display driving circuit of the timepiece may be of the order of 1KHz.

Preferably the display of the timepiece is of the luminous crystal or of the light emitting diode type.

The invention is illustrated in and further explained in connection with the accompanying drawings in which:

Figure 1 is a block diagram of a timepiece embodying the invention;

Figure 2 is a schematic representation of the construction of one form of monolithic integrated circuit in accordance with the invention; and

Figure 3 is an explanatory graphical figure. Referring to Figure 1, block 1 represents a time standard oscillator, block 2 is a frequency divider for dividing the relatively high frequency from the oscillator 1 to a relatively low frequency and block 4 is a driving circuit for driving a time display—e.g. a luminous

crystal time display. The parts 1 and 2 are supplied with one operating voltage and the part 4 is supplied with a higher operating voltage—as illustrated 1.5V and 3.0V respectively. Between parts 2 and 4 is an interposed part 3 which will be described later herein and to which both operating voltages are supplied. Parts 1, 2 and 4 are as known per se and require no description herein. Part 3 is provided in accordance with this invention.

If a monolithic integrated circuit is supplied from two operating power supplies of different voltages there is the practical difficulty that if the two supplies are to have a common terminal, as is, of course, normally the case, the circuit elements which are supplied with different potentials from the remaining supply terminals must be insulated from one another. In the case of a monolithic integrated circuit using an N-type substrate, this difficulty is overcome, in accordance with the invention, by connecting the elements which are supplied with the higher potential to the said common terminal (i.e. by making the said common terminal the terminal of highest potential), separating the other P-type islands, and supplying them with the appropriate lower potentials from the lower potential terminals of the supply. In a monolithic integrated circuit with C-MOS elements, a P-channel transistor is formed on an N-type substrate, and an N-channel transistor is formed by a P-type island.

Figure 2 is a schematic representation of an actual construction. On an N-type substrate (N-sub) are formed two P-type islands (P-tub 1) and (P-tub 2). N-type diffused areas (N) and P-type diffused areas (P) are inserted into the substrate as indicated so that sources S_1 , S_2 , S_3 and S_4 and drains D_1 , D_2 , D_3 and D_4 are formed in the positions indicated, there being thus four transistors as indicated at Tr_1 , Tr_2 , Tr_3 and Tr_4 . The drains D_1 and D_2 and the drains D_3 and D_4 are respectively coupled so as to be common to each other. Each pair of transistors Tr_1 and Tr_2 , Tr_3 and Tr_4 constitutes a complementary inverter, M_1 and M_2 being metal electrodes for the gates. It will be seen that each of the sources is connected with a substrate on which each is formed, P-type islands (P-tub 1) and (P-tub 2) being formed on the N-type substrate (N-Sub). The substrate (N-Sub) is connected with the portions supplied from the common highest potential terminal and the P-type islands (P-tub 1) and (P-tub 2) are connected with the portions supplied from the two lower potential terminals. Because the islands (P-tub 1) and (P-tub 2) are reverse biased with respect to the substrate (N-Sub), the said islands are insulated from one another electrically and it is for this reason that they can be supplied with different potentials.

The C-MOS inverter is composed of a pair

of P-channel and N-channel MOS transistors. The relation between the drain voltage and the gate voltage of the C-MOS inverter is shown graphically in Figure 3. When the threshold voltages V_{GTN} and V_{GTP} of the N-channel and the P-channel transistors are nearly equal, the gate switching voltage V_{GO} of this inverter is nearly half of the supply voltage V_{DD} .

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$$V_{GO} \approx \frac{1}{2} V_{DD}$$

Accordingly, in the case of C-MOS integrated circuit operated from two different voltages, the difference occurs in a so-called logic level and consequently it is not possible directly to transmit a signal from one to the other of the component circuits embodied in the structure. It is therefore necessary to provide an interface for adapting the logic levels to one another. Block 3 of Figure 1 accordingly includes means providing an interface for this purpose.

As will now be appreciated the invention offers substantial practical advantages and is particularly (though not exclusively) advantageous for use in electronic timepieces. When applied to an electronic timepiece it offers the advantage that a relatively low operating voltage can be used for the oscillator (2) and the frequency divider (3)—with consequent higher reliability and lower breakdown voltage—even though a higher voltage is required for the driving circuit (4). In the case illustrated in Figure 1, the voltage for the oscillator and divider is only half that used for the driving circuit. Moreover the power consumption is low and the invention lends itself well to miniaturisation and the use of a very small chip. By employing the invention to provide, in an electronic timepiece, a monolithic integrated circuit structure with portions operated by different voltages it is possible to make the electronic circuitry of the timepiece very small indeed, of relatively low power consumption and of relatively low cost. The advantages of the invention, especially that of relatively low power consumption, are especially outstanding in the case of a timepiece having a time display of the liquid crystal or of the luminous diode type.

WHAT WE CLAIM IS:—

1. An electronic circuit structure composed of complementary MOS transistors, and comprising a circuit portion requiring a relatively high operating supply voltage and a circuit portion requiring a relatively low operating supply voltage, wherein said circuit portions are

of monolithic integrated circuit construction and are connected, one to the other, through a signal interface which adapts the logic levels of said portions to one another.

2. A structure as claimed in claim 1 wherein there are C-MOS elements constituting P-channel and N-channel transistors, the former being formed on an N-type substrate and the latter being formed by P-type islands on said substrate.

3. A structure as claimed in claim 2 wherein P-type areas are formed on the substrate and N-type diffusions are formed therein to provide transistor drains and sources, the drains of each pair of those transistors which are adjacent to one another being respectively coupled so as to be common to each other and metal electrodes are provided to constitute gates for the transistors, the arrangement being such that each transistor source is connected with the substrate on which it is formed.

4. Monolithic integrated circuit structures substantially as herein described with reference to Figures 2 and 3 of the accompanying drawings.

5. An electronic timepiece including, in the electronic circuitry thereof, a structure as claimed in any of the preceding claims.

6. A timepiece as claimed in claim 5 wherein that circuit portion of the integrated circuit structure which requires the relatively high voltage is employed for the driving circuit for driving the time display of the timepiece.

7. A timepiece as claimed in claim 5 or 6 wherein circuit portions of the integrated circuit structure requiring the relatively low voltage are employed for the time standard oscillator of the timepiece and for the frequency divider provided therein for dividing the oscillator frequency down to a relatively low frequency for the time display driving circuit of the timepiece.

8. A timepiece as claimed in claim 6 or 7 wherein the input frequency to the time display driving circuit of the timepiece is of the order of 1KHz.

9. A timepiece as claimed in any of claims 5 to 8 wherein the display of the timepiece is of the luminous crystal or of the light emitting diode type.

10. Electronic timepieces substantially as herein described.

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