A MULTIPROCESSOR PROGRAMMABLE INTERRUPT CONTROLLER SYSTEM WITH PROCESSOR-INTEGRATED INTERRUPT CONTROLLERS

ABSTRACT OF THE DISCLOSURE

A multiprocessor programmable interrupt controller (MPIC) system has an interrupt bus, distinct from the system (memory) bus, for handling interrupt request (IRQ) related messages. Each processor chip has an on-board interrupt acceptance unit (IAU) coupled to the interrupt bus for the acceptance of IRQs and for broadcasting of IRQs generated by its associated on-chip processor. I/O device interrupt lines are connected to one or more interrupt delivery units (IDUs) that are each coupled to the interrupt bus for broadcasting of I/O-generated IRQs. The interrupt bus is a synchronous three-wire bus having one clock wire and two data wires for 2-bit parallel-serial data transmission. Arbitration for control of the interrupt bus by the IAUs and IDUs uses one of the data wires. Lowest priority IRQ delivery mode uses a similar one-wire arbitration procedure for determining which IAU has the lowest current priority task running in its associated on-chip processor. A modification to the lowest priority mode arbitration procedure also provides means for uniform distribution of IRQs to eligible processors. The actual servicing of the IRQs is done by means of the system bus.

A MPIC cluster system provides a means for interconnecting individual MPIC systems into an expanded interrupt controller system whenever the interrupt handling capacity of an individual MPIC system (cluster) is exceeded by using a cluster manager.

(Figure 2)