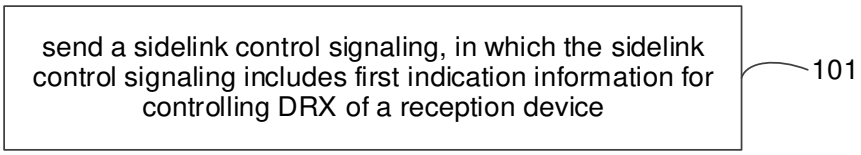


FIG. 1

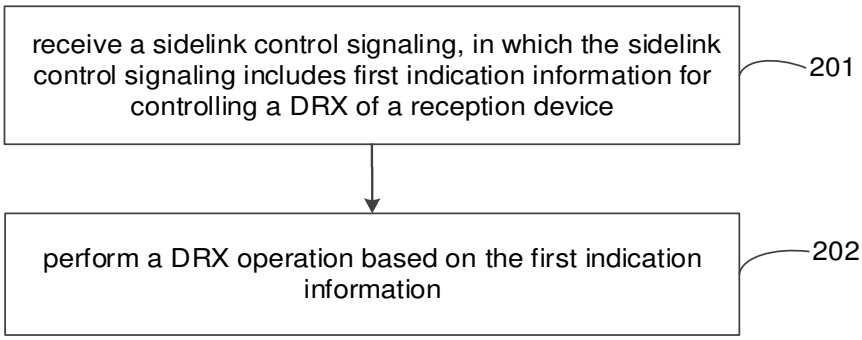


FIG. 2

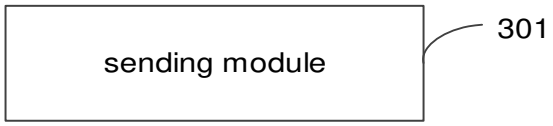


FIG. 3

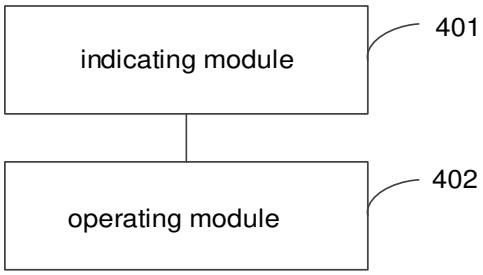


FIG. 4

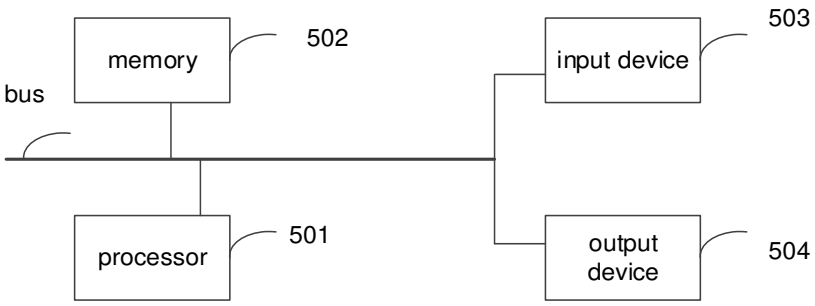
memory
502
input device
503
bus
processor
501
output device
504

**FIG. 5**