What is claimed is:

1. A resistive type memory device comprising:

a plurality of banks, each bank comprising a bank row decoder connected to a plurality of word lines of the bank, a bank column decoder connected to a plurality of bit lines of the bank, and a memory cell bank array having memory cells arranged in a plurality of rows and columns, each row of memory cells connected to a corresponding one of the word lines and each column of memory cells being connected to a corresponding one of the bit lines, the memory cells of each bank being organized in a plurality of tiles, each of the memory cells comprising a variable resistor that is programmable to store at least one bit of data;

an address register configured to provide a sequence of memory addresses, each memory address including a bank address identifying one of the plurality of banks, a row address identifying a word line location within the bank identified by the bank address and a column address identifying a subset of bit lines connected to the word line identified by the row address;

a control circuit configured to provide each row address and column address of each memory address stored by the address register respectively to the bank row decoder and column decoder of the bank identified by the bank address of the corresponding memory address;

wherein, for at least each memory address of a subset of the memory addresses, the control circuit is configured to modify ~~at least one of~~ the corresponding row address and the corresponding column address such that ~~at least one of~~ the following is true:

a relative location of a first word line identified by a first row address within a first bank of the plurality of banks is different from a relative location of a second word line identified by the first row address within a second bank of the plurality of banks, and

relative locations of first bit lines identified by a first column address within a first bank of the plurality of banks is different from corresponding relative locations of second bit lines identified by the first column address within a second bank of the plurality of banks.

~~2. The resistive type memory device of claim 1,~~

~~wherein, for the subset of the memory addresses, the control circuit is configured to modify the corresponding row address so that the relative location of the first word line identified by the first row address within the first bank of the plurality of banks is different from the relative location of the second word line identified by the first row address within the second bank of the plurality of banks.~~

~~3~~2. The resistive type memory device of claim 1~~ or claim 2~~,

wherein the first word line is located in a first area of the first bank and the second word line is located in a second area of the second bank,

wherein the first area comprises memory cells having a higher resistance distribution degradation than memory cells of the second area.

~~4~~3. The resistive type memory device of claim ~~3~~2, wherein the first area is located at an edge of the first bank and the second area is located at a center of the second bank.

~~5~~4. The resistive type memory device of claim ~~3~~2, wherein the first area is located at an edge of a horizonal block of memory tiles of the first bank through which the first word line extends and the second area is centrally located in a horizontal block of memory tiles of the second bank through which the second word line extends.

~~6~~5. The resistive type memory device of any one of claims 1 to ~~5~~4,

wherein, with respect to the first bank, a sequence of row addresses in numerical order from the lowest row address of the sequence to the highest row address of the sequence sequentially identifies word lines from a first edge of the first bank to a second edge of the first bank, and

wherein, with respect to the second bank, the sequence of row addresses in numerical order from the lowest row address of the ~~range~~sequence to the highest row address of the ~~range~~sequence sequentially identifies word lines in locational order from a center of the second bank to a first edge of the second bank and then from a second edge of the first bank to ~~a~~ the center of the second bank.

~~7~~6. The resistive type memory device of any one of claims 1 to ~~5~~4,

wherein, with respect to the first bank, a sequence of row addresses in numerical order of a range of row addresses from the lowest row address of the range to the highest row address of the range sequentially identifies word lines in locational order arranged from a first edge of a first tile of the first bank to a second edge of the first tile of the first bank, and

wherein, with respect to the second bank, the sequence of row addresses in numerical order of the range from the lowest row address of the range to the highest row address of the range sequentially identifies word lines in locational order from a center of a first tile of the second bank to a first edge of the first tile of the second bank and then from a second edge of the first tile of the second bank to ~~a~~ the center of the first tile of the second bank.

~~8~~7. The resistive type memory device of any one of claims 1 to ~~7~~6, wherein the control circuit comprises an address modification circuit configured to invert at least one of the more significant bits of all of the row addresses of the subset of the memory addresses.

~~9~~8. A resistive type memory device comprising:

a plurality of banks, each bank comprising a bank row decoder connected to a plurality of word lines of the bank, a bank column decoder connected to a plurality of bit lines of the bank, and a memory cell bank array having memory cells arranged in a plurality of rows and columns, each row of memory cells connected to a corresponding one of the word lines and each column of memory cells being connected to a corresponding one of the bit lines, the memory cells of each bank being organized in a plurality of tiles, each of the memory cells comprising a variable resistor that is programmable to store at least one bit of data;

an address register configured to provide sequence of memory addresses, each memory address including a bank address identifying one of the plurality of banks, a row address identifying a word line location within the bank identified by the bank address and a column address identifying a subset of bit lines connected to the word line identified by the row address;

a control circuit configured to provide each row address and column address of

each memory address stored by the address register respectively to the bank row decoder and column decoder of the bank identified by the bank address of the corresponding memory address;

wherein, for at least each memory address of a subset of the memory addresses, the control circuit is configured to modify at least one of the corresponding row address and the corresponding column address such that at least one of the following is true:

a relative location of a first word line identified by a first row address within a first bank of the plurality of banks is different from a relative location of a second word line identified by the first row address within a second bank of the plurality of banks, and

relative locations of first bit lines identified by a first column address within a first bank of the plurality of banks is different from corresponding relative locations of second bit lines identified by the first column address within a second bank of the plurality of banks,

wherein, for the subset of the memory addresses, the control circuit is configured to modify the corresponding column address so that relative locations of the first bit lines identified by the first column address within the first bank of the plurality of banks are different from corresponding relative locations of second bit lines identified by the first column address within the second bank of the plurality of banks.

~~10~~9. The resistive type memory device of claim ~~9~~8,

wherein memory cells connected to the first bit lines have a higher resistance distribution degradation than memory cells connected to the second bit lines.

~~11~~10. The resistive type memory device of claim ~~9~~ 8 or claim ~~10~~9, wherein the first bit lines are located at an edge of the first bank and the second bit lines are located at a center of the second bank.

~~12~~11. The resistive type memory device of claim ~~9~~ 8 or claim ~~10~~9,

wherein the tiles of each bank are arranged in columns to form corresponding bays of tiles,

wherein the first bit lines are arranged at corresponding edges of corresponding bays of the first bank and the second bit lines are arranged at central locations of

corresponding bays of the second bank.

~~13~~12. A method of storing data comprising:

forming a first codeword from a first block of data;

storing the first codeword in a resistive type memory device so that a first portion of the first codeword is stored in ~~a~~ first resistive type memory cells of the resistive type memory device and a second portion of the first codeword is stored in second resistive type memory cells of the resistive type memory device, the storing the first codeword in the resistive type memory device comprising:

sending a write command to the resistive type memory device to store the first codeword in the resistive type memory device,

sending a first memory address associated with the write command to the resistive type memory device, the memory address including a first row address and a first column address, and

sending the first codeword to the resistive type memory device,

wherein the first resistive type memory cells are identified by the first row address and first column address within a first bank of the resistive type memory device,

wherein the second resistive type memory cells are identified by the first row address and first column address within a second bank of the resistive type memory device, and

wherein the first resistive type memory cells have a first relative location with respect to the first bank,

wherein the second resistive type memory cells have a second relative location with respect to the second bank, and

wherein the first relative location is different from the second relative location.

~~14~~13. The method of claim ~~13~~12,

wherein the first resistive type memory cells are connected to a first word line of the first bank that is identified by the first row address within the first bank, the first word line being formed at the first relative location with respect to the first bank, and

wherein the second resistive type memory cells are connected to a second word line of the second bank that is identified by the first row address within the second bank, the second word line being formed at the second relative location with respect to the second

bank.

~~15~~14. The method of claim ~~14~~13,

wherein each of the first bank and the second bank comprise a plurality of resistive type memory cells organized in a plurality of tiles, the plurality of tiles of each bank being organized in a plurality of bays of tiles,

wherein the first word line is located within a first tile of the first bank at a first relative location with respect to the first tile,

wherein the second word line is located within a second tile of the second bank at a second relative location with respect to the second tile, and

wherein the first relative location is different from the second relative location.

~~16~~15. The method of claim ~~15~~14, wherein the first relative location with respect to the first tile is located adjacent an edge of the first memory tile and the second relative location with respect to the second tile is centrally located within the second tile.

~~17~~16. The method of any one of claims ~~13~~ 12 to ~~16~~15,

wherein the first resistive type memory cells are connected to a first set of bit lines of the first bank that is identified by the first column address within the first bank, and

wherein the second resistive type memory cells are connected to a second set of bit lines of the second bank that is identified by the first column address within the second bank.

~~18~~17. The method of claim ~~17~~16,

wherein each of the first bank and the second bank comprise a plurality of resistive type memory cells organized in a plurality of tiles, the plurality of tiles of each bank being organized in a plurality of bays of tiles,

wherein the first set of bit lines are respectively located within corresponding bays at edges of the corresponding bays of the first bank, and

wherein the second set of bit lines are centrally located within corresponding bays of the ~~first~~ second bank.

~~19~~18. The method of any one of claims ~~13~~ 12 to ~~18~~17, further comprising:

receiving information data from a host;

dividing the information data into blocks of data, including the first block of data;

performing error correction encoding operations on each of the blocks of data to generate a plurality of corresponding codewords, the plurality of codewords including the first codeword, each codeword including a corresponding one of the blocks of data and corresponding parity bits generated from a corresponding error correction encoding operation; and

storing the plurality of codewords in the resistive type memory device so that first portions of each of the plurality of codewords are stored in the first bank of the resistive type memory device and second portions of each of the plurality of codewords are stored in the second bank,

wherein, for each of the plurality of codewords, a relative location of resistive type memory cells storing the first portion of the codeword within the first bank is different from a relative location of resistive type memory cells storing the second portion of the codeword within the second bank.

~~20~~19. The method of claim ~~19~~18, wherein the first portion and second portion of each of the plurality of codewords is identified by a same corresponding row address and same corresponding column address.