CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a memory array region comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells;

an additional control logic region overlying the stack structure and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells;

conductive pad structures underlying the stack structure and electrically connected to the control logic devices;

additional conductive pad structures overlying the stack structure and electrically connected to the additional control logic devices; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures.

2. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages less than or equal to about 1.4 V.

3. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages within a range of from about 0.7V to about 1.3 V.

4. The microelectronic device of claim 1, wherein the control logic devices and the additional control logic devices each individually comprise CMOS circuitry.

5. The microelectronic device of claim 1, further comprising:

conductive line structures vertically between the stack structure and the additional conductive pad structures;

conductive routing structures vertically between the conductive line structures and the additional conductive pad structures; and

interconnect structures vertically between the conductive routing structures and the additional conductive pad structures.

6. The microelectronic device of claim 5, wherein:

the conductive routing structures comprise aluminum; and

the interconnect structures comprise copper.

7. A microelectronic device, comprising:

a memory array region comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells;

an additional control logic region overlying the stack structure and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells; and

an additional memory array region underlying the control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional vertically extending strings of memory cells within the additional stack structure.

8. A method of forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

conductive pad structures electrically connected to the control logic devices;

a stack structure over the conductive pad structures and comprising vertically alternating conductive structures and insulating structures;

additional conductive pad structures overlying the stack structure;

vertically extending strings of memory cells within the stack structure; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices; and

attaching the first microelectronic device structure to the second microelectronic device structure such that the stack structure vertically intervenes between the control logic region and the additional control logic region, and such that the additional conductive pad structures are electrically connected to the additional control logic devices.

9. The method of claim 8, further comprising selecting the additional control logic devices to comprise CMOS circuitry configured to operate at applied voltages within a range of from about 0.7 V to about 1.4 V.

10. The method of claim 9, further comprising selecting the control logic devices to comprise additional CMOS circuitry configured to operate at other applied voltages greater than the applied voltages effective to operate of the CMOS circuitry of the additional control logic devices.

11. A method of forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices;

attaching the first microelectronic device structure to the second microelectronic device structure such that the stack structure vertically intervenes between the control logic region and the additional control logic region;

forming a third microelectronic device structure comprising:

a further control logic region comprising further control logic devices; and

an additional memory array region over the further control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional vertically extending strings of memory cells within the additional stack structure; and

attaching the third microelectronic device structure to the first microelectronic device structure such that the additional stack structure vertically underlies the stack structure.