SUBSTRATE FOR STRESSED SYSTEMS AND METHOD FOR CRYSTAL GROWTH ON SUCH A SUBSTRATE

Field of the invention and prior art

The invention relates to the field of substrates for crystal growth (epitaxial growth) and to techniques for crystal growth using said substrates.

It is applicable to techniques for epitaxial growth of layers of materials such as GaN, GaAs, InP, GaAlAs, InGaAs, AlN, AlGaN, or even SiGe.

Attempts are currently being made to produce epitaxial layers of those materials, in particular in the case of gallium nitride GaN. In particular, relatively thick layers (> 1 or 2 μm) are required with good crystal qualities, which are not stressed or are only slightly stressed, and which have low defect densities (for example with a dislocation density of less than $10^6/cm^2$).

A known example of epitaxial growth is that of GaN using the MOCVD technique to obtain thick layers of GaN (> 12 micrometers (μm)) on a substrate for epitaxy.

The literature mentions epitaxial growth of that type essentially on the following bulk substrates: sapphire, SiC, and Si. Those three substrates are the most frequently used, since they are the most readily available substrates. A few tests have been carried out on substrates such as ZnO or $LiGaO_2$.

Currently, epitaxial GaN layers homogeneously deposited on a substrate surface have a dislocation density in the range 10^8 and $10^{10}/cm^2$ regardless of the nucleation surface used.

The stresses in thick GaN layers obtained by MOCVD (growth temperature 1000-1100°C) clearly depend on the coefficient of thermal expansion of the epitaxial substrate, which determines the stresses of thermoelastic origin that are imposed on the system.

GaN layers produced on sapphire are in compression, while those obtained on SiC are under slight tension and

those on silicon are under high tension. For layers under tension, this results in a strong tendency to form cracks in the epitaxial film, thereby destroying it. The layers in compression are also a problem.

That phenomenon is particularly true for growth on silicon. For that epitaxy support, the limit beyond which cracks appear is about 1 μm to 2 μm, which is a limiting factor as regards producing good quality layers.

Growth tests on SOI (silicon on insulator) substrates have shown that the use of that type of substrate can reduce the crystal defect density in the epitaxially grown layer because of the compliant nature of the very thin film of silicon present on the oxide. However, that system is limited in its capacity to absorb stresses, in particular for thick GaN layers (at best 1 μm to 2 μm).

Crystal quality appears to be improved by growth on substrates having motifs. The dislocation densities obtained are of the order of $10^6/cm^2$. Epitaxial lateral overgrowth (ELO) techniques exist, along with techniques known as pendeoepitaxy (PE), lateral overgrowth from trenches (LOFT), and cantilever epitaxy (CE). All of those techniques are based on lateral overgrowth and coalescence of the epitaxially grown layer to ultimately form a continuous film. The continuous films obtained have precise zones with improved crystal quality (the epitaxial lateral overgrowth (ELOG) technique), or have a homogeneous film of crystal quality (LOFT technique). Those solutions have been demonstrated for sapphire, SiC, and Si (111).

Although they improve the crystal quality of the epitaxially grown film, those solutions cannot effectively solve the problem of stress in the epitaxially grown films.

Thus, there is a problem with producing a substrate or a support that can absorb a high level of stresses during crystal growth, in particular during thick

epitaxial growth of a material, and in particular in the case in which the coefficient of thermal expansion of the material is different or very different from that of the substrate or the epitaxy support.

There is also the problem with finding a substrate or a support that can absorb high levels of stresses, in particular to obtain thick layers, for example when growing GaN layers.

Description of the invention

In a first aspect, the invention provides a support for crystal growth comprising:

- a nucleation or growth layer;
- a polycrystal, porous, or amorphous buffer layer or intermediate layer; and
- a base substrate.

The buffer layer can absorb or accommodate stresses appearing during epitaxial growth carried out on the nucleation or growth layer of the support.

This novel type of support can thus more readily produce epitaxial layers with a thickness of the order of a few µm, for example 4 µm, in particular thick GaN layers.

The nucleation layer can be a layer of monocrystalline material, for example formed from Si or SiC or GaN, or formed from sapphire or AlN or diamond. It can be obtained by transfer from another substrate.

The support substrate can be formed from Si or SiC, and the buffer layer can be formed from amorphous silicon, porous silicon, polysilicon, amorphous silicon dioxide SiO_2, amorphous silicon nitride Si_3N_4, silicon carbide (SiC), gallium nitride (GaN), sapphire or aluminum nitride (AlN).

In a variation, the nucleation layer is formed from silicon, the buffer layer is polycrystal or porous, the base substrate is formed from silicon, and an

electrically insulating layer is also included between the nucleation layer and the buffer layer.

The insulating layer can then be a layer of oxide (for example of silicon) or a boro-phospho-silicate glass layer.

The structure of the invention is compatible with SOI (silicon on insulator) type structures.

Thus, in a first implementation of the invention, an intermediate layer is formed between the base substrate and either the nucleation layer or the SOI double layer (superficial silicon layer and insulating layer, for example silicon oxide).

In a further implementation of the invention, mechanical absorption means or a mechanical system is formed on the base substrate that can absorb thermoelastic stresses generated at the surface.

This mechanical system comprises, for example, an array of absorbing elements, which can be obtained by machining the base substrate, e.g. by ionic etching.

The invention also provides a support for crystal growth comprising at least one nucleation or growth layer and a base substrate into which motifs are etched.

The nucleation layer and the base substrate can be formed from silicon, an oxide or electrically insulating layer being located between the nucleation layer and the substrate.

This second implementation is therefore also compatible with an SOI type structure.

A buffer layer can be located between the nucleation or growth layer or the oxide layer and the base substrate, said buffer layer being porous or polycrystal, for example, for example formed from Si, amorphous silicon, porous silicon, polysilicon, SiC, GaN, sapphire or AlN.

An epitaxial growth method in accordance with the invention can be carried out on a support in accordance with the invention, as defined above.

Brief description of the figures

- Figures 1 and 2 show a first implementation of the invention;
- Figures 3A to 4 show a second implementation of the invention;
- Figures 5A and 5B show steps of a substrate fracture method.

Detailed description of implementations of the invention

In a first implementation, a buffer or intermediate layer is interposed between a nucleation or growth layer and a base substrate, which buffer layer can absorb a quantity of stresses, for example by generating crystalline defects in said layer or by mechanical displacement of material in said layer.

One example of said structure is shown in Figure 1, which shows a nucleation layer 2, a buffer layer 4 as mentioned above, and a support substrate 6 such as Si or SiC or sapphire (Al_2O_3) or aluminum nitride (AIN).

The buffer layer 4 is a polycrystal, porous, or amorphous layer, for example. It can be formed by CVD technique and can be formed from silicon (Si), silicon carbide (SiC), gallium nitride (GaN), sapphire or aluminum nitride (AlN), silicon dioxide (SiO_2), or silicon nitride Si_3N_4. Said materials are given by way of example.

In the example of the silicon layer, the buffer layer can be a thin layer of amorphous silicon, polysilicon or porous silicon (obtained by intentional porosification or by porous deposit).

The nucleation layer 2 is, for example, a layer of monocrystalline material, obtained by transferring a thin layer from a first substrate, for example using the fracture method known as "Smart-Cut" (see Figures 5A and 5B relating to this subject, or even the article by A. J. Auberton-Hervé cited below in this description).

Typically, the thickness of the nucleation layer is of the order of 0.1 µm to 2 µm thick, for example 0.5 µm; the thickness of the buffer layer is of the order of a few tenths of µm, for example about 0.01 µm to about 1 µm or 2 µm, and the substrate can be of the order of several hundred µm, or in the range 100 µm to 700 µm, for example about 500 µm or 525 µm.

The coefficients of thermal expansion C_1 and C_2 of the nucleation layer 2 and of the substrate 6 can be different. For example, SiC has a coefficient of thermal expansion of $4.5\times10^{-6}K^{-1}$, Si has a coefficient of $2.5\times10^{-6}K^{-1}$, alumina (Al_2O_3) has a coefficient of $7\times10^{-6}K^{-1}$.

This difference in the coefficients of the layer 2 and of the substrate 6 can generate stresses during phases of temperature rise or fall, in particular once the relative difference $|C_1 - C_2|/C_1$ or $|C_1 - C_2|/C_2$ is at least 10% or 20% or 30% at ambient temperature, i.e. about 20°C or 25°C.

In that type of structure, stresses generated during an excursion in temperature are absorbed by the buffer layer 4. In the case of a polycrystal layer, the stresses are absorbed therein by defect generation. In the case of a porous layer, the pores allow local displacement of material which mechanically absorb the tensions or stresses. In the case of an amorphous layer, the privileged relaxation mode of the stresses occurs by creep of the layers present.

The invention is also applicable to an SOI type structure in which the oxide is not an oxide of silicon, but an oxide which becomes viscous at a lower temperature, for example a boro-phospho-silicate glass (BPSG). If the layer is viscous, it absorbs the tensions and stresses by creep.

That same type of buffer layer can be interposed in an SOI structure between the oxide or insulating layer and the substrate. Such a structure is shown in Figure 2, in which reference number 10 designates a thin layer

of semiconductive material, preferably monocristalline, e.g. formed from silicon, silicon carbon SiC, gallium nitride GaN, sapphire, or AIN. Reference number 12 designates a layer of SiO_2 oxide, layer 14 represents the buffer layer and reference number 16 represents a substrate formed from a semiconductive material, e.g. thick silicon.

In such an SOI structure, the oxide layer also acts as a stress accommodation layer because the crystal growth methods are carried out at temperatures of the order of several hundred degrees (for example: 1000°C). At those temperatures, the oxide becomes viscous and absorbs some of the stresses. The buffer layer 14 will also absorb some of said stresses, but in a different manner as it does not become viscous.

The relative difference in the coefficient of thermal expansion between the nucleation layer 10 and the substrate 16 can therefore, likewise, be greater than 10% or 20% or 30% at ambient temperature (20°C or 25°C).

For an SOI structure, the buffer layer 14 can, for example, result from a deposit of amorphous or polycrystal silicon that can box in and absorb stresses and is, for example, in the range 10 nm to 1 µm or 0.1 µm to 2 µm thick.

Typically, the thickness of the layer 10, which can be formed by transfer, is about 10 nm to 300 nm, or is even in the range 0.1 µm to 2 µm. The thickness of the layer 12, which can be formed by deposit, is of the order of a few hundred nm, for example in the range 100 nm to 700 nm, for example 400 nm.

The substrate 10 can be of substantially the same thickness as the substrate 6 in Figure 1.

In a further implementation shown in Figure 3A, in a substrate 20 or rigid support, an accommodation layer 22 is generated which is elastic or which has a certain elasticity at least in a plane xy, parallel to the plane of the different layers 24, 26. Said layer 22, is

obtained, for example, by etching notches or trenches or any other geometric motif into the substrate 20. Said motifs have an elasticity or are flexible in a plane parallel to the plane of layers 24, 26. The resulting elasticity can be calculated by applying the conventional beam theory.

In a variant, shown in Figure 3B, a resilient accommodation layer 23, similar to that in Figure 3A, can also be formed in the rear face of the substrate 20, thereby preventing possible problems of adherence between the layer 26 and the substrate 20 which can appear in the configuration in Figure 3A. This variant can also absorb stresses.

The two mechanical stress accommodation systems in Figures 3A and 3B can be present in the same substrate.

In another variant (Figure 3C), notches 25 such as "saw-cuts", for example, are made in the substrate 20 on one or both sides of the substrate. Once again, a stress absorption effect is obtained.

It is also possible to have a system such as that in Figure 3A or 3B on one side of the substrate, and a system such as that in Figure 3C on the other side.

The etched or hollowed out motifs preferably repeat themselves in a two-dimensional periodic pattern or in one dimension as shown in Figure 4.

As an example, trenches with a depth p equal to about 10 µm, and with a width ℓ = 1 µm and spaced apart by an amount e = 1 µm, are hollowed into the substrate 20 to generate said mechanical absorption system.

The layers 24, 26 and the substrate 20 can be identical or similar to layers 2, 4 and to the substrate 6 of Figure 1, with the same typical thicknesses, and obtained with the same techniques. The nucleation layer 24 can, for example, be a layer of monocrystalline material obtained by transferring a thin layer from a first substrate, for example using the "Smart Cut" method or by fracturing the substrate (the steps of said method

being described below in connection with Figures 5A and 5B), and the buffer layer 26 can, for example, be a polycrystal or porous layer of Si, SiC, GaN, sapphire or AlN.

The structure of Figures 3A, 3B, or 3C can also be a structure of the SOI type, the layer 26 being a layer of oxide or insulator and the layer 24 being a fine layer of silicon.

It is also possible to carry out these implementations using a structure such as that shown in Figure 2, the substrate 16 being etched on one and/or the other of the faces parallel to the plane of the layers 10, 12, 14 to form an elastic accommodation layer as described above with reference to Figures 3A to 3C.

In Figure 3A, if the support is obtained by molecular bonding of the layer 26 to the substrate 20, carrying out bonding onto a substrate with trenches may modify the bonding step, in particular since the surface area brought into contact may be substantially reduced (by about 50%, for example).

In addition, in the case of highly etched surfaces (and thus with a small contact surface area or a very reduced contact surface area), for example, the distribution of the trenches or of the notches could be optimized to allow spontaneous bonding. To this end, the geometric parameters of the patterns could be adjusted, e.g. the width and/or the periodicity of said patterns.

In order to obtain an etched substrate and to be able to preserve a flat bonding surface, it is possible to obturate the surface of the substrate in part or completely prior to bonding. Even complete obturation over the entire depth of the trenches or of the etched patterns enables an absorption effect of the stresses to be conserved.

In one example, if the surface is formed from silicon, a step for smoothing the surface of the substrate 20 in a stream of hydrogen can be carried out

to close the etching pits in part or completely by migration of silicon atoms, as illustrated in Figure 4, in which reference number 28 indicates filling of a trench with silicon over a certain depth h.

In a further example, a non-conforming material (for example an oxide) is deposited to obturate the trenches at the surface. Said deposit can be carried out by a non-optimized shallow trench isolation (STI) filling method. Such a method is, for example, described in C. P. Chang et al. "A highly manufacturable corner rounding solution for 0.18 µm shallow trench insulation", IEMD 97-661.

The assembled support forms an element that can mechanically absorb stresses by movement and/or deformation of the bars or notches or the walls of the trenches under the effect of the thermoelastic stress.

The method known under the name "smart-cut" (or substrate fracture) is described in the article by A. J. Auberton-Hervé et al. "Why can Smart Cut change the future of microelectronics?", published in International Journal of High Speed Electronics and Systems, Vol. 10, No. 1, 2000, P. 131-146.

Steps of that method are described below with reference to Figures 5A and 5B, in which the references 40 and 42 designate two substrates, both formed from semiconductive materials, for example.

In a first step (Figure 5A), ionic or atomic implantation is carried out into the substrate 40, forming a thin layer 52 which extends substantially parallel to the surface 41 of the substrate 40. A layer or plane of weakness or fracture is formed, defining in the volume of the substrate 40 a lower region 45 intended to constitute a thin film and an upper region 44 constituting the bulk of the substrate 40. Hydrogen is generally implanted, but other species can also be implanted, including co-implantation of hydrogen and helium.

The substrate 42 is provided with engraved patterns, for example, as described above. Engraving is performed from the surface 43 and/or from the surface 47.

The two substrates 40 and 42 so prepared are then assembled with face 43 against face 41 using a wafer bonding technique (assembling wafers using any technique that is known in the microelectronics field) or by adhesive contact (e.g. molecular adhesion) or by bonding. With regard to these techniques, reference could be made to the work by Q. Y. Tong and U. Gösele, "Semiconductor Wafer Bonding", (Science and Technology), Wiley Interscience Publications.

A portion 44 of the substrate 40 is then removed by a thermal or mechanical treatment that causes a fracture along the plane of weakness 52. An example of that technique is described in the above-mentioned article by A. J. Auberton-Hervé et al.

The structure obtained is that shown in Figure 5B.

In order to reinforce the bonding interface or the join between the substrate 42 (or its face 43) and the thin layer 45 (or the contact face 41), it may be desirable to raise the temperature to about 1000°C.

During the different temperature rise phases, the structure of the motifs etched in the substrate 42, in particular their flexibility or elasticity, compensates for or absorbs the stresses and the variational differences due to differences between the coefficients of the thermal expansion of the two substrates 40, 42. The relative difference between said coefficients can, as already mentioned above, be at least 10% or at least 20% or at least 30% at ambient temperature.

The film 45 can also be a nucleation or growth layer such as the layer 2, 10, or 24 in Figures 1 to 3C (the substrate 42 being similar to the substrate 6, 16, 20 in Figures 1 to 4). However, unlike those structures, the structure in Figure 5B does not present a buffer layer.

The film 45 can also be replaced by an assembly of superimposed films. In other words, this aspect of the invention not only concerns a monolayer on substrate system, but any multilayer system that employs layers deposited on a substrate. It is, for example, the association of the nucleation layer and the buffer layer in Figures 1 to 3C.

The formation of a plane of weakness can be obtained by methods other than ion implantation. Thus, it is also to make a layer of porous silicon, as described in the article by K. Sataguchi et al. "ELTRAN® by Splitting Porous Si layers", Proceedings of the 9th International Symposium on Silicon-on-Insulator Tech. and Device, 99-3, the Electrochemical Society, Seattle, p. 117-121 (1999).

Other techniques also enable the substrates to be thinned without implementing ion implantation and without creating a plane of weakness: such techniques include polishing and etching.

CLAIMS

1. A support for crystal growth comprising:
   - a nucleation layer (2, 10);
   - a polycrystal, porous, or amorphous buffer layer (4, 14); and
   - a support substrate (6, 16).

2. A support according to claim 1, in which the nucleation layer (2) is a layer of monocrystalline material.

3. A support according to claim 2, in which the monocrystalline material is formed from silicon, silicon carbide (SiC), gallium nitride (GaN), sapphire, aluminum nitride (AlN), or diamond.

4. A support according to any one of claims 1 to 3, in which the nucleation layer (2) is obtained by transfer from another substrate.

5. A support according to any one of claims 1 to 4, in which the support substrate (6, 16) is formed from silicon (Si), silicon carbide (SiC), sapphire, aluminum nitride (AIN), or diamond.

6. A support according to any one of claims 1 to 5, in which the buffer layer is formed from silicon, amorphous silicon, porous silicon, polysilicon, silicon carbide, gallium nitride, sapphire, aluminum nitride, or silicon nitride.

7. A support according to any one of claims 1 to 6, in which the nucleation layer (10) is formed from silicon, the buffer layer (14) is polycrystal or porous, the support substrate (16) is formed from a semiconductive layer, and a layer (12) of oxide is included between the nucleation layer and the buffer layer (14).

8. A support according to claim 7, in which the oxide layer is a layer of a thermal or deposited oxide of silicon or a layer of boro-phospho-silicate glass (BPSG).

9. A support according to any one of claims 1 to 8, in which the thickness of the nucleation layer is in the range 0.1 μm to 2 μm.

10. A support according to any one of claims 1 to 9, in which the thickness of the buffer layer is in the range 0.01 μm to 2 μm.

11. A support according to any one of claims 1 to 10, further comprising motifs (22, 23, 25, 43) etched or formed into the support substrate (6, 26).

12. A support for crystal growth, comprising at least one nucleation layer (24), and a support substrate (6, 16) in which motifs (22, 23, 25, 43) are etched or formed or produced, said motifs having elasticity, or being flexible in a plane parallel to the nucleation layer.

13. A support according to claim 12, in which the nucleation layer and the support substrate are formed from silicon, and a layer of oxide or insulator is located between the nucleation layer and the substrate.

14. A support according to claim 12 or claim 13, further comprising a buffer layer (4, 14) or intermediate layer, located between the nucleation layer (24) or the layer of oxide or insulator, and the support substrate.

15. A support according to claim 14, in which the buffer layer is polycrystal or porous.

16. A support according to claim 15, in which the buffer layer is formed from silicon or amorphous silicon, porous silicon, polysilicon, silicon carbide (SiC), gallium nitride (GaN), sapphire, aluminum nitride (AlN), or silicon nitride.

17. A support according to any one of claims 11 to 16, the patterns being etched or formed or produced in, or from, the face (43) of the substrate facing the nucleation layer, and/or in, or from, the face (47) of the substrate opposite the face facing the nucleation layer (2, 10, 24).

18. A support according to any one of claims 11 to 16, patterns being etched or formed or produced in, or starting from, the face (43) of the substrate facing the nucleation layer, and being obturated in part or completely at the surface (43) of the support substrate.

19. A support according to any one of claims 11 to 18, in which the motifs are in the form of notches, trenches, or saw-cuts.

20. An epitaxial growth method in which growth is carried out on a support according to any one of claims 1 to 19.

21. A method according to claim 20, the material which is grown being formed from GaN, GaAs, InP, GaAlAs, InGaAs, AIN, AlGaN or SiGe.