

MULTI-CORE HETEROGENEOUS SOC, DEBUGGING METHOD FOR MULTI-CORE HETEROGENEOUS SOC, ELECTRONIC DEVICE, AND STORAGE MEDIUM

ABSTRACT

Disclosed are a multi-core heterogeneous SoC, a debugging method for the SoC, an
electronic device, and a storage medium. The SoC is provided with a USB device and integrates a
plurality of heterogeneous systems. A first virtual UART serial port in the heterogeneous system
establishes a binding relationship with target USB endpoints in the USB device connected to a
USB host disposed in a debugging device. A second virtual UART serial port in the debugging
device and corresponding to the heterogeneous system establishes a binding relationship with the
target USB endpoints in the USB device through the USB host. The SoC is configured to transmit
debugging data corresponding to the heterogeneous system with the debugging device through the
USB device and the USB host based on the first virtual UART serial port, the target USB
endpoints, and the second virtual UART serial port in the debugging device.

(FIG. 1)