Method for detection of digitally transmitted data

Technical field

The invention relates to a method for detection of digitally transmitted data, with received symbols first of all being equalized in a decision feedback equalizer which has, in a manner known per se, a feedforward filter, a decision maker and a feedback filter, and these symbols then being decoded by a decoder. The invention also relates to a circuit arrangement for carrying out the method.

Prior art

The liberalization of telecommunications has led to a search for opportunities to provide a broadband transmission via existing cables and media which are not primarily designed for data transmission. Of particular interest is the use of the electricity power cable grid since, so to speak, this grid system is already connected to every household. In other words: the transmission medium already exists and just needs to be used in a suitable way.

The problem of electrical cables is that powerful pulsed interference exists (which is typically caused by switching processes). Other interference sources (echoes, radiated interference etc.) also make it harder to transmit broadband signals.

Description of the invention

The object of the invention is to specify a method of the type mentioned initially which is suitable for the detection of signals in an environment

subject to powerful, in particular pulsed, interference.

The object is achieved by the features defined in claim 1. According to the invention, in a first phase, the symbols are processed in a manner known per se by a DFE (decision feedback equalizer) and the decoder. In a subsequent, second phase, the symbols are tapped off from the output side of the decoder and are fed back to the feedback filter, excluding the decision maker contained in the DFE. In other words, the feedback no longer takes place within the DFE but includes the channel decoder.

The error statistics at the output from the DFE are bursty. This means that the errors are no longer distributed more or less uniformly, but appear in clusters. This is due to the fact that incorrect decisions from the output of the DFE are (also) fed back to the feedback filter, and remain in the equalizer for some time. They thus influence subsequent decisions. The de-interleaver at the output of the DFE distributes the errors uniformly and results in symbols which are adjacent at the input of the decoder having a tendency to be uncorrelated. In general, a lower error rate can be expected on the output side of the decoder. The fed-back symbols are in general more reliable than those which are generated within the DFE by the decision maker. In a corresponding way, the result of the second phase is normally better than that of the first.

The second phase is preferably carried out a number of times. The symbols or symbol sequences thus pass through the decoder a number of times. The output signal from the feedforward filter need not be recalculated, but can be taken from the first phase. The evaluation process is terminated on reaching a suitable selected criterion.

A first option is for the variance in the reliability at the output of the decoder to be determined in each run, and for the feedback to be ended as soon as no more improvement occurs (that is to say as soon as the symbol decisions no longer change).

The calculation loop can in any case be terminated when an error check code contained in the received signal (for example a cyclic redundancy code CRC) is satisfied.

It is also possible to predetermine the number of recursions. In this case, too many runs may be carried out if the interference is weak, and too few if it is strong. However, the advantage of this method is that the computation time is known in advance and there is no need to evaluate any complex termination criteria.

The evaluation process in the decoder can be improved by using so-called a-priori information from previous iterations for decoding the symbols in the current iteration. In the course of soft-decision decoding, for example, a reliability value exists for each symbol estimate. This value, which is determined in a manner known per se, is used according to the invention to improve the estimation in the decoder.

The method according to the invention can be implemented without any difficulties using known means (ASICs, processors, memory elements etc.). Specifically, the method is suitable for transmission of digital signals with a high bandwidth (1 Mbit/s or more) via electrical power distribution lines in the area of the end user ("last mile"). However, it is in no way limited to this application.

Further advantageous embodiments and feature combinations of the invention result from the following detailed description and the totality of the patent claims.

Brief description of the drawing

In the drawing used to explain the exemplary embodiment:

Figure 1 shows a block diagram of a receiver according to the invention.

Ways to implement the invention

Figure 1 shows the general structure of the part of the receiver which processes the data. The (previous) demodulation of the received signal is not shown. The symbol and frame synchronization are not the subject matter of the invention, either. It is thus assumed that the corresponding method steps have already been carried out.

The data from a symbol sequence are thus present at the input of a feedforward filter 1. In a first phase, these data are equalized using a DFE. This means that the intersymbol interference produced by the channel is corrected. Apart from the feedforward filter 1, the DFE comprises, in a manner known per se, a decision maker 3 and a feedback filter 5. Figure 1 also shows a switch 4 between the decision maker 3 and the feedback filter 5. In the first phase, this is set such that the output of the decision maker 3 is passed to the feedback filter 5. An adder 2 subtracts the data supplied from the feedback filter 5 from the output signal from the feedforward filter 1.

The filter coefficients of the two filters are calculated, and the decision is made in the decision maker 3, in a manner known per se.

The output from the adder 2 is passed to a de-interleaver 6. This changes the symbol sequence in such a way that originally adjacent symbols are no longer

next to one another. The errors, which are not distributed uniformly at the output from the DFE but occur virtually in bursts, are in consequence distributed over the symbol stream. This is inconsistent with the assumption by the decoder 7 that the errors occur randomly distributed.

The downstream decoder 7 cancels out the channel coding (produced in the transmitter, which is not shown) so that the transmitted data can be extracted. The channel coding is not part of the invention either. This can be carried out in any suitable way.

In contrast to the normal receiver structures, feedback from the output of the decoder 7 via the interleaver 8 to the feedback filter 5 is provided in this structure. The interleaver 8 reverses the interleaving of the de-interleaver 6. The switch 4 is set in a second phase so as to allow the desired feedback of the decoded symbols. The decision maker 3 no longer has any function in the second phase.

The entire method sequence (namely the switching of the switch 4 and the satisfaction of the termination criterion in the second phase) is monitored by a symbolically illustrated controller 10.

The data are detected as follows:

During a first run (first phase), the switch 4 is in the position shown in Figure 1. The DFE thus carries out the equalization process, the de-interleaver 6 interleaves the symbols, and the decoder 7 eliminates the channel coding. In the process, the signal supplied from the feedforward filter 1 is preferably stored. (For example, a FIFO memory can be provided between the feedforward filter 1 and the adder 2. This FIFO memory is filled once in the first phase, and is read from at the same time, and is then just read from a number of times successively in the second

phase. In other words: the feedforward filter 1 is not required in the second phase.)

The switch 4 is moved to the other position in order to carry out the second phase. The stored values of the feedforward filter 1 are output a number of times and are passed through the processing loop (de-interleaver 6, decoder 7, interleaver 8, feedback filter 5).

According to one particularly preferred embodiment, a-priori information is available in a memory 9. This information (for example reliability values for individual symbols from previous iterations) can be used to reduce the error rate in the decoder 7.

The number of iterations may, for example, be preset to a fixed value. However, a measure may also be calculated which indicates the increase in reliability of the symbol decisions between successive iterations. If there is no increase, or only a minor increase, the iteration is terminated. For packet-oriented transmission, satisfaction of the integrated CRC (cyclic redundancy check) may also be used as a termination criterion. Other possibilities are, of course, not precluded. In this case, a number of individual criteria may be combined by logic "and" or "or" operations. Example: "Terminate the iterations if the error check code is satisfied or when a certain number of iterations have been carried out."

In the SNR (signal-to-noise ratio) area of interest, the error rate at the output of the decoder 7 is less than at its input. If a convolution code is used and if the decoder 7 is a sequence estimator, the error at the output from the decoder 7 may once again be in the form of bursts (for example if a convolution code and a maximum likelihood sequence estimator are used). However, the interleaver 8 will reduce the correlation even in this case.

The described receiver structure is very general since it does not demand either a specific interleaver or a specific decoder. If the decoder is a soft-decision decoder, there is complete freedom to decide which soft-decision information from the DFE output is used for decoding. The principles for use of a-priori information in a decoder in the area of so-called turbo-decoding are known (see, for example, B.C. Berrou, A. Glavieux and P. Thitimajshima, "Near Shannon-limit error-correction coding and decoding, turbo codes", Proc.ICC '93, pp. 1064-1079, Geneva, May 1993) and can be used for the receiver structure according to the invention.

The decoder may be a sequence estimator or a symbol estimator (MAP decoder). In the latter case, the sequence which is fed back can be produced by renewed coding of the estimated information symbols.

The sequence fed back to the feedback filter may, instead of this, comprise symbol decisions, for reliability reasons ("soft feedback").

Although the transmitter is matched to the receiver (that is to say it has a channel coder and an interleaver which correspond to the de-interleaver 6 and the decoder 7), no further special features are otherwise required.

The receiver structure according to the invention is typically used in conjunction with digital data transmission by modulation of a single carrier signal. The channel characteristic may be time and/or frequency selective.

In summary, it can be stated that the invention can be used for receivers which have a DFE with a downstream de-interleaver and a channel decoder in the digital part. The processing is carried out iteratively and generally allows the reliability of the estimated symbols to be improved.

Patent Claims

1. A method for detection of digitally transmitted data, with received symbols first of all being equalized in a decision feedback equalizer which has, in a manner known per se, a feedforward filter (1), a decision maker (3) and a feedback filter (5), and these symbols then being decoded by a decoder (7), characterized in that - after a first run through the decision feedback equalizer - the data supplied from the decoder (7) are fed back to the feedback filter (5) in the course of a postprocessing phase and excluding the decision maker (3).

2. The method as claimed in claim 1, characterized in that the postprocessing phase comprises a number of iterations until a predetermined termination criterion is satisfied.

3. The method as claimed in claim 2, characterized in that the iterations are terminated when the variance in the symbol reliability no longer changes significantly between successive iterations.

4. The method as claimed in claim 2 or 3, characterized in that the iterations are terminated when a check code integrated in the received signal is satisfied.

5. The method as claimed in one of claims 2 to 4, characterized in that a predetermined number of iterations are carried out.

6. The method as claimed in one of claims 1 to 5, characterized in that the decoder (7) uses a-priori information based on previous iterations.

7. Use of the method as claimed in claim 1 for detection of data transmitted via power supply lines.

8. A circuit arrangement for carrying out the method as claimed in claim 1, comprising a decision feedback equalizer which, in a manner known per se, has

a feedforward filter (1), a decision maker (3) and a feedback filter (5), and comprising a decoder (7), characterized in that feedback is provided from the decoder (7) to the feedback filter (5) in order - after a first run through the decision feedback equalizer - to process the data supplied from the decoder (7) in the course of a postprocessing phase and excluding the decision maker (3).

9. The circuit arrangement as claimed in claim 8, characterized in that a de-interleaver (6) is provided upstream of the decoder (7), and an interleaver (8) is provided in the feedback.