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(54) Title: DUAL CONTACT AND POWER RAIL FOR HIGH PERFORMANCE STANDARD CELLS

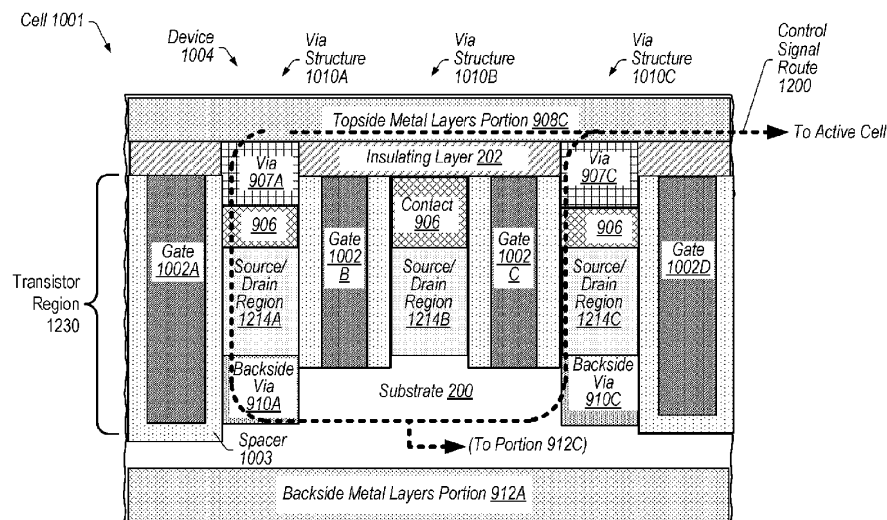


FIG. 12

(57) Abstract: Standard cell layouts that may be implemented in FinFET devices or nanosheet FET devices is disclosed. The standard cell layouts include power supply connections from both a topside metal layer and a backside metal layer. A device in a standard cell may be connected to both the topside metal layer and the backside metal layer. Various cell layouts may include a control signal route that passes from a first device into backside layers and then underneath a second device. Various implementations of backside and topside routing of bitlines and wordlines in memory arrays are also disclosed.

[Continued on next page]

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