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(54) CIRCUIT ARRANGEMENT FOR GENERATING A CONTROL SIGNAL FOR THE FIELD OUTPUT STAGE IN A TELEVISION RECEIVER

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a circuit arrangement for producing a control signal for the field output stage in a television receiver suitable for the reception of line and field synchronizing pulses, a number of fields constituting an image, the arrangement comprising a generator for generating a signal of line frequency or an integral multiple thereof, a frequency divider circuit receiving the generated signal, and means for applying received field synchronizing pulses to a comparison stage for comparing the phase between these pulses and the pulses generated by the frequency divider circuit, the comparison stage being capable of applying a signal to a gate which signal is dependent on the phase difference between the compared pulses. Such a circuit arrangement is capable of being switched between internal and external field synchronization.

Such a circuit arrangement is described in Netherlands Patent Application 7101894. Since in this known circuit arrangement the control signal is derived from the line synchronizing signal by means of frequency division, the frequency thereof is correct as soon of the line synchronizing circuit has control over the frequency which is generally effected fairly quickly. The correct phase of the field control signal obtained relative to the field sychronizing pulses originating from the transmitter and received by the television receiver is insured by the comparison stage which may be formed as a coincidence gate, and an integrator. When the inputs to this gate do not coincide the comparison stage provides a plurality of pulses so that the integrator supplies a signal after a given period whch enables the gate. The frequency divider circuit is then reset: this is direct synchronization in which the generated control signal is directly influenced by the received sychronizing pulses. The phase is then correct, the comparison stage no longer provides pulses and the received synchronizing pulses can in principle no longer reach the divider circuit, at least not as long as the signal generated by the circuit arrangement maintains the same frequency and same phase as the received pulses: this is indirect synchronization in which the received synchronizing pulses cannot directly influence the generated control signal.

It is an object of the invention to provide a circuit arrangement which is also suitable for the reception of "non-standard signals" which are signals in which the number of lines per image deviates from the number prescribed in the relevant television system. Such signals are generated by some test signal generators in which the displayed image is not interlaced and which are used, for example, for adjusting the convergence in colour television receivers or may be produced when using video recorders, for example, for the display of still pictures. Field synchronization with the known circuit arrangement may not be possible when such signals are received, for the frequency of the received field synchronizing pulses deviates from the frequency of the pulses obtained by division so that a vertical roll-over is obtained. Some received synchronizing pulses reset, however, the frequency divider circuit so that the image occasionally jumps in the vertical direction.

The invention provides a circuit arrangement of the type to which the invention relates, and further comprises a gating pulse generator for generating first and second gating pulses, the frequency divider circuit

being reset during the occurrence of the first gating pulse when the compared pulses do not subsist coincidentally and means for applying the second gating pulses to an automatic selection circuit which selection circuit switches the circuit arrangement to produce the control signal from the divided pulses when the compared pulses subsist coincidentally, and switches the circuit arrangement to produce the control signal from the received pulses when the compared pulses do not subsist coincidentally during the occurrence of the second gating pulse.

The above and other features of the invention will be described in greater detail by way of example with reference to the accompanying drawing in which:—

Figure 1 shows a block-schematic diagram of a television receiver provided with the circuit arrangement according to the invention.

Figure 2 shows details of the circuit arrangement according to the invention,

Figures 3, 4 and 5 show waveforms which occur in the circuit arrangement of Figure 2.

In Figure 1, 1 is an aerial by which a television signal can be received. This signal is applied to an RF and detection section 2. The detected signal subsequently reaches the audio section 3 of the television receiver and a video amplifier 4 at the output of which a complete video signal, possibly with a chrominance signal in the case of colour television, is available. This signal is applied to a section 5 in which it is processed for application to a picture display tube 6, the signal also be applied to a sync. separator 7. The output voltage of the sync. separator 7 includes line sychronizing pulses which are applied to a phase detector 8 whose output voltage can influence an oscillator 11 through a flywheel filter 9 and a reactance circuit 10. Oscillator 11 generates a voltage at twice the line freqeuncy $2f_H$, i.e. 31250 Hz upon reception of a signal in accordance with the television system using 625 lines per complete image, 2 interlaced fields per image and 50 fields per second. The oscillator 11 may alteratively generate a voltage at the line frequency f_H whose frequency is subsequently doubled. The voltage at the frequency $2f_H$ controls a frequency divider circuit 12 in which its frequency is divided by two and the signal thus obtained is applied through a pulse shaper 13 to the line output stage 14 which provides the line deflection current for the deflection coil (not shown) for the horizontal deflection of the electron beam(s) in tube 6.

The voltage available at the output of oscillator 11 is also applied to a generator 15 of field frequency signals in which its frequency is divided by 625 and is further processed. When oscillator 11 has the correct frequency after pulling-in in frequency of the circuit 8, 9, 10, 11 for indirect line synchronization, the frequency of the signal generated by generator 15 is also correct, that is to say, it is equal to the field frequency in the mentioned standard of 50 Hz. A pulse shaper 17 receives the signal generated by generator 15 and controls a field output stage 18 which applies the field deflection current to the deflection coil (not shown) for the vertical deflection of the electron beam(s) in tube 6. Both the line and the field control signals have the waveforms required for stages 14 and 18 due to the two pulse shapers 13 and 17, respectively. If the output signal of divider circuit 12 or generator 15 has already this shape, pulse shapers 13 and 17, respectively, may be omitted.

The output voltage of sync separator 7 also includes field synchronizing pulses which are separately obtained by means of a field sync. separator 19 and are subsequently applied to an input of a coincidence gate 20. The divided pulses originating from an output of generator 15 are applied to a second input of gate 20. In the coincident or in-phase state that is to say, in the case where a field synchronizing pulse originating from separator 19 and a divided pulse subsist coincidentally, stage 20 does not provide a signal at its output. In the non coincident or out of phase state where the pulses do not subsist coincidentally it provides a signal, namely the divided pulse, for an integrator 21 which is followed by a level detector 22. When this state lasts approximately 0.4 s which corresponds to approximately 20 field pulses, the detected level exceeds a given threshold value so that a signal is applied to an input of an AND gate 16. The field synchronizing pulses at the output of separator 19 reach an input of an OR-gate 25 through a controlled switch 23 which can be rendered conducting by the output signal from gate 16. The same gate output signal is also applied to generator 15.

A further input of gate 16 is connected to an output of an automatic selection circuit 26 while the output signal from gate 25 is applied in a manner to be described hereinafter to generator 15 and to circuit 26. The output signal from pulse shaper 17 is also applied to a pulse generator 27 having two outputs one of which is connected to an input of gate 25 whilst the other is connected to an input of circuit 26. The divided pulses which are applied to coincidence stage 20 are also applied to an input of selection circuit 26 while another input thereof as well as another input of generator 15 receives the pulses originating from separator 19.

A control signal for the field output

stage 18 is generated by generator 15 with the aid of pulse generator 27 and selection circuit 26. This control signal always has the correct frequency and the correct phase after a short pull-in period irrespective of whether the field synchronizing pulses received from separator 19 are standard signals or not. This will be explained with reference to Figure 2 in which elements 15, 26 and 27 of Figure 1 are shown in greater detail.

Generator 15 includes a frequency divider circuit 29 which in known manner, for example, by means of bistable elements, divides the frequency $2f_H$ of the signal generated by oscillator 11 by 625. As is known ten bistable elements must be present so that the output signal from circuit 29 has a natural frequency of $\frac{2f_H}{2^{10}}$ which corresponds to a natural period of approximately 33ms. Circuit 29 is internally reset after a field period i.e. approximately 20 ms after the commencement of the period, i.e. $20 - \frac{33}{2} \approx 3.5$ ms after reversal in the middle of the natural period. A pulse shaper 30 reduces this flyback pulse to approximately 300 μs which is slightly longer than the field synchronizing pulse provided by separator 19 and whose duration is approximately 200 μs. These pulses are compared in coincidence stage 20. The output signal from pulse shaper 30 also reaches through a first controlled switch 31 and a NOR-gate 32. A further input of gate 32 receives through a second controlled switch 33 the output signal from separator 19. The output signal from gate 32 serves as a trigger signal for an oscillator 34 formed in known manner which provides the output signal of generator 15. Switch 33 can be rendered conducting by the output signal from gate 16 while the same signal can render switch 31 conducting through an inverter stage 35. Finally the reset terminal (S_2) of divider circuit 29 is connected to the output of gate 25.

Pulse generator 27 includes an auxiliary frequency divider circuit 36 which may be a counter and by which the repetition frequency in this example 50 Hz of its input signal (Figure 3a) is divided by an integer n. In this example n is equal to 16, so that the output signal from circuit 36 has a period of $n \times 20 = 16 \times 20 = 320$ ms and has the shape as is shown in Figure 3b. This signal is applied to a gating pulse shaper 37 which generates in known manner two series of gating pulses of the same repetition frequency as that of the signal in Figure 3b. The first gating pulse (Figure 3c) is applied to gate 25 and has a duration of approximately 20 ms, that is to say approximately one field period. It is generated for example by a monostable element which is responsive to a trailing edge of the signal in Figure 3b. The second gating pulse (Figure 3d) has approximately the same duration as the first but occurs a given number of field periods later, in this example $n - 1 = 15$, so that its lagging edge coincides with the leading edge of the next first gating pulse. The second gating pulse is applied to an input of an OR gate 38 forming part of the automatic selection circuit 26. In Figure 3a the field frequency pulses are shown to be very narrow. In practice they have a given duration so that one of these pulses coincides with one of the pulses of Figure 3c and Figure 3d. The pulses of Figures 3c and 3d may alternatively be shifted in such a manner that they commence and end in the period located between two of the field frequency pulses of Figure 3a.

The divided pulses from pulse shaper 30 and the synchronizing pulses from separator 19 are applied to other inputs of gate 38. The outputs of gate 38 and of gate 25 are connected to the set (S_1) and reset terminals (S_2), respectively, of a flipflop 39 whose Q-output is connected to an input of gate 16.

Oscillator 34 is a free-running oscillator, for example an astable multivibrator, which receives trigger pulses through the gate 32. Figure 2 shows that these pulses originate from either separator 19 (direct sychronization), or from frequency divider circuit 29 (indirect synchronization), which will now be described in greater detail.

With coincidence at stage 20 the level detector 22 does not apply a signal to gate 16 which may be indicated by the binary digit 1. During the occurence of the second gating pulse all input signals to gate 38 coincide at least partly which coresponds to the digit 0 for each input. Under these circumstances the output signal from gate 38 is also 0, that is to say, a set pulse is applied to terminal S_1 of flipflop 39 so that the output signal Q thereof is 1. The output signal from gate 16 is therefore 1 with the result that switches 23 and 33 are open with switch 31 closed. The divided pulses are applied through gate 32 to oscillator 34. One of the inputs of gate 25 conveys the signal 1, the output signal thereof is consequently 1: neither divider circuit 29 nor flipflop 39 can be reset. As long as the coincidence state prevails, with every second gating pulse at gate 38 and level detector 22 providing the signal 1, the situation shown is maintained while the generated control signal cannot be influenced by the received synchronizing pulses.

When the out of coincidence state occurs, level detector 22 provides after approxi-

mately 0.4s a signal which is equal to 0 for gate 16. The output signal thereof becomes 0 so that switches 23 and 33 are closed while switch 31 is opened. The synchronizing pulses received from separator 19 are applied through gate 32 to oscillator 34 while the divided pulses cannot influence this oscillator (direct synchronization). The generated control signal is then synchronous with the received signal, but as is shown the duration of this state must be short due to the higher sensitivity to interference of the circuit at least when receiving broadcasting television signals. This is effected as follows. Since the first gating pulse from pulse generator 27 occupies approximately one field period a synchronizing pulse will occur during a first gating pulse. Both inputs of gate 25 are therefore equal to 0 so that the output thereof is also 0. Frequency divider circuit 29 is reset. Since there is a lack of coincidence in gate 38 the output signal thereof is equal to 1. This is the signal at the terminal S_1 of flipflop 39 while terminal S_2 receives a 0. Flipflop 39 is thus reset: Q becomes 0, but circuit 26 has no influence on the rest of the circuit because level detector 22 provides a signal which is equal to 0 for gate 16.

When the incoming signals are standard signals, the above-described situation continues, while the divided pulses and the synchronizing pulses are always in phase, until the occurrence of the next second gating pulse from pulse generator 27. During this occurrence the three input signals of gate 38 are equal to 0 so that a reset pulse 0 is applied to the terminal S_1 of flipflop 39: Q becomes 1. The input signals for coincidence stage 20 coincide from the beginning of direct synchronization so that both input signals for gate 16 become equal to 1 at the instant when Q = 1. The output signal from gate 16 thus becomes 1 so that switches 23 and 33 are opened and switch 31 closes. Consequently the received signal does not reach the oscillator 34 while the divided pulses are applied to this oscillator (indirect synchronization). Nothing is changed in the state of divider circuit 29 because the output signal from switch 23 and consequently that from gate 25 becomes equal to 1 so that circuit 29 and flipflop 39 are not reset.

After the occurence of the second gating pulse the output signal from gate 38 becomes equal to 0, but this does not change the state of flipflop 39. During the next second gating pulse a set pulse is applied to flipflop 39 but the output signal Q thereof was already 1 and thus does not change. The foregoing shows that the time which elapses until indirect synchronization occurs is as long as the time interval between the occurence of the first and second gating pulses, i.e. in the described example $(n-1) \times 20 = 15 \times 20 = 300$ ms after the out of coincidence state is established, i.e. approximately 0.4 s after its occurence, increased by the time which is necessary for coincidence of a synchronizing pulse with a first gating pulse. Since the divisor corresponding to the incoming synchronizing pulses will not deviate in practice very much from 625 the latter period will last not more than a period of the first gating pulse, i.e. 320 ms. This is the reason why both gating pulses have a duration of approximately one field period. When this duration is shorter it is possible that coincidence is not effected even when receiving standard signals so that the circuit never pulls in. On the other hand too long a duration might render the circuit more sensitive to interference. Figure 3 shows that a duration of approximately one field period can simply be realized.

When the incoming signals are not standard signals the circuit behaves in a different manner. Since divider circuit 29 is reset during the occurrence of the first gating pulse the two input signals for coincidence stage 20 coincide at least once. It is however uncertain whether this happens more than once and what is the output signal from level detector 22. This, however, has no influence on the manner of sychronization: in fact the divided pulse and the synchronizing pulse do not occur simultaneously during the occurrence of the second gating pulse so that the output signal Q from flipflop 39 remains equal to 0 and hence those of gates 16 and 25 also remain 0 independent of the situation in stage 20. As long as non-standard signals are received the synchronization of oscillator 34 thus remains direct which is no drawback because the signal generated by test signal generators and video recorders generally include little noise and interference.

Divider circuit 29 is reset at each first gating pulse. When the incoming signal is a standard signal, the divided pulses and the synchronizing pulses are in phase. At the next second gating pulse coincidence is effected in gate 38 so that the circuit is immediately switched over to indirect synchronization, otherwise a new cycle of n field periods will start. Another function of resetting divider switch 29 every time is the following. When receiving non-standard signal the time difference between the divided and the synchronizing pulses would increase without this step, with the risk that coincidence might take place in gate 38 at an arbitary instant so that unwanted indirect synchronization might be the result.

After the divided pulse and the synchronizing pulse have coincided during the occurrence of the first gating pulse a time difference which increases with each period

is produced between these pulses upon reception of non-standard signals. Since the period of the signal generated by oscillator 11 is $\frac{1}{2f_H} \approx 32$ μs, this difference after one field period is equal in μs to $32 \times (625-d)$ where d is the divisor of the incoming signal deviating from 625. The number n must be chosen to be such that the time difference $(n-1) \times 32 \times (625-d)$ can be observed by gate 38 after $n-1$ periods. Figure 4a shows a synchronizing pulse and Figure 4b shows a divided pulse which pulses have the stated duration of approximately 200 μs and in an extreme case of the coincident state this is the state at which the two leading edges coincide. Figure 4c shows the extreme case of the non coincident state which might occur subsequently and which is the state at which the leading edge of the synchronizing pulse coincides with the trailing edge of the divided pulse. Figures 5a, 5b and 5c show the opposite situation. Figures 4a, 4b, 4c, and 5a, 5b and 5c show that the above-mentioned time difference must be in the order of 300 μs. The number n is thus determined by the condition $n-1 \geq \frac{300}{32(625-d)}$ which proves that the more the divisor d deviates from 625 the less n may be. When for the sake of security the smallest possible difference $625-d = \pm 1$ is chosen, i.e. d is 624 or 626, a value is found for n which is at least equal to 11. Auxiliary frequency divider circuit 36 might in principle divide the field frequency by 11, but it is simpler to divide by 16, for example, by means of four binary elements, for example, flipflops. As a result the pull-in time is slightly extended relative to the case where $n = 11$, namely 300 ms instead of $10 \times 20 = 200$ ms, but it is still acceptable while the reliability and the insenstivity to interference are also increased.

The foregoing shows that the output signal Q from the automatic selection circuit 26 is equal to 0 in the non coincident state and becomes 1 after some time when standard signals are received so that synchronization is first effected directly and then indirectly. When receiving non-standard signals Q remains equal to 0 so that direct sychronization is maintained.

It will be noted that the gating pulses in Figures 3c and 3d succeed each other after $n-1$ field periods so that the lagging edge of one pulse coincides with the leading edge of the other. It will be evident that this is not of essential importance, that is to say, a given time may elapse between these edges. Nor is it necessary for auxiliary frequency divider circuit 36 to divide the frequency of the signal from pulse shaper 17 and not, for example, that from oscillator 34 or from divider circuit 29. Oscillator 34 may be omitted in the case where the output signal from gate 32 has the correct waveform to control pulse shaper 17. In the embodiment of Figure 2 the gating pulses are obtained by means of the auxiliary frequency divider cicuit 36. A different method is alternatively possible, namely by the integration of the pulses of Figure 3a. By means of suitable pulse shapers gating pulses can then be obtained whose repetition frequency is not necessarily equal to the field frequency divided by an integer such as is the case with circuit 36.

Negative logic is used in the foregoing description, that is to say, logic in which 0 means "signal" and 1 means "no signal". It is obvious that this choice is not important for the essence of the invention. With positive logic only the terms for the logic gates shown in Figures 1 and 2 would have to be changed in known manner.

Elements 10 to 13, 15 to 17 and 20 to 27 of the described circuit, except for a capacitor optionally assocaited with integrater 21 may advantageously be integrated in a semiconductor body. In view of the large number of components thereof it is obvious that a non-integrated embodiment would not be economical. It may be noted that the described embodiment includes binary elements. Embodiments of the same scope as in the present application are, however, feasible in which different elements may be used.

A television system using 625 lines per image, 2 interlaced fields per image and 50 fields per second has been used hereinbefore as an example of a standard system. It will be evident that modifications of the circuit according to the invention are possible without essential difference for the reception of television signals in accordance with a different system.

WHAT WE CLAIM IS:—

1. A circuit arrangement for producing a control signal for the field output stage in a television receiver which receiver is suitable for the reception of line and field synchronizing pulses, a plurality of fields constituting an image, said arrangement comprising a generator for generating a signal line frequency or an integral multiple thereof, a frequency divider circuit for producing divided pulses from said generated signal, means for applying received field synchronizing pulses to a comparison stage for comparing the phase between said received pulses and said divided pulses, said comparison stage being adapted to apply a signal to a gate which signal is dependent on the phase difference between the com-

is produced between these pulses upon reception of non-standard signals. Since the period of the signal generated by oscillator 11 is $\frac{1}{2f_H} \approx 32\ \mu s$, this difference after one field period is equal in μs to $32 \times (625-d)$ where d is the divisor of the incoming signal deviating from 625. The number n must be chosen to be such that the time difference $(n-1) \times 32 \times (625-d)$ can be observed by gate 38 after $n-1$ periods. Figure 4a shows a synchronizing pulse and Figure 4b shows a divided pulse which pulses have the stated duration of approximately 200 μs and in an extreme case of the coincident state this is the state at which the two leading edges coincide. Figure 4c shows the extreme case of the non coincident state which might occur subsequently and which is the state at which the leading edge of the synchronizing pulse coincides with the trailing edge of the divided pulse. Figures 5a, 5b and 5c show the opposite situation. Figures 4a, 4b, 4c, and 5a, 5b and 5c show that the above-mentioned time difference must be in the order of 300 μs. The number n is thus determined by the condition $n-1 \geq \frac{300}{32(625-d)}$ which proves that the more the divisor d deviates from 625 the less n may be. When for the sake of security the smallest possible difference $625-d = \pm 1$ is chosen, i.e. d is 624 or 626, a value is found for n which is at least equal to 11. Auxiliary frequency divider circuit 36 might in principle divide the field frequency by 11, but it is simpler to divide by 16, for example, by means of four binary elements, for example, flipflops. As a result the pull-in time is slightly extended relative to the case where $n = 11$, namely 300 ms instead of $10 \times 20 = 200$ ms, but it is still acceptable while the reliability and the insenstivity to interference are also increased.

The foregoing shows that the output signal Q from the automatic selection circuit 26 is equal to 0 in the non coincident state and becomes 1 after some time when standard signals are received so that synchronization is first effected directly and then indirectly. When receiving non-standard signals Q remains equal to 0 so that direct sychronization is maintained.

It will be noted that the gating pulses in Figures 3c and 3d succeed each other after $n-1$ field periods so that the lagging edge of one pulse coincides with the leading edge of the other. It will be evident that this is not of essential importance, that is to say, a given time may elapse between these edges. Nor is it necessary for auxiliary frequency divider circuit 36 to divide the frequency of the signal from pulse shaper 17 and not, for example, that from oscillator 34 or from divider circuit 29. Oscillator 34 may be omitted in the case where the output signal from gate 32 has the correct waveform to control pulse shaper 17. In the embodiment of Figure 2 the gating pulses are obtained by means of the auxiliary frequency divider cicuit 36. A different method is alternatively possible, namely by the integration of the pulses of Figure 3a. By means of suitable pulse shapers gating pulses can then be obtained whose repetition frequency is not necessarily equal to the field frequency divided by an integer such as is the case with circuit 36.

Negative logic is used in the foregoing description, that is to say, logic in which 0 means "signal" and 1 means "no signal". It is obvious that this choice is not important for the essence of the invention. With positive logic only the terms for the logic gates shown in Figures 1 and 2 would have to be changed in known manner.

Elements 10 to 13, 15 to 17 and 20 to 27 of the described circuit, except for a capacitor optionally assocaited with integrater 21 may advantageously be integrated in a semiconductor body. In view of the large number of components thereof it is obvious that a non-integrated embodiment would not be economical. It may be noted that the described embodiment includes binary elements. Embodiments of the same scope as in the present application are, however, feasible in which different elements may be used.

A television system using 625 lines per image, 2 interlaced fields per image and 50 fields per second has been used hereinbefore as an example of a standard system. It will be evident that modifications of the circuit according to the invention are possible without essential difference for the reception of television signals in accordance with a different system.

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1. A circuit arrangement for producing a control signal for the field output stage in a television receiver which receiver is suitable for the reception of line and field synchronizing pulses, a plurality of fields constituting an image, said arrangement comprising a generator for generating a signal line frequency or an integral multiple thereof, a frequency divider circuit for producing divided pulses from said generated signal, means for applying received field synchronizing pulses to a comparison stage for comparing the phase between said received pulses and said divided pulses, said comparison stage being adapted to apply a signal to a gate which signal is dependent on the phase difference between the com-

pared pulses, a gating pulse generator for generating first and second gating pulses, said frequency divider circuit being reset during the occurrence of said first gating pulse when said compared pulses do not subsist coincidentally, and means for applying said second gating pulse to an automatic selection circuit which selection circuit switches the circuit arrangement to produce said control signal from said divided pulses when said compared pulses subsist coincidentally, and switches the circuit arrangement to produce said control signal from said received pulses when said compared pulses do not subsist coincidentally during the occurrence of the said second gating pulse.

2. A circuit arrangement as claimed in Claim 1, in which the repetition rate of said gating pulses is equal to the repetition rate of the pulses generated by the frequency divider circuit divided by an integer *n*, each second gating pulse occuring a number of field periods after a first gating pulse.

3. A circuit arrangement as claimed in Claim 2, in which the pulse length of each of said gating pulses is approximately one field period.

4. A circuit arrangement as claimed in Claim 1, in which said automatic selection circuit includes a gating device and a bistable element, means for applying the field synchronising pulses, the divided pulses generated by the frequency divider circuit and the second gating pulses to said gating device, the output of said gating device being connected to said bistable element, and means for deriving an output signal therefrom to form a second input signal for the gate associated with said comparison stage.

5. A circuit arrangement as claimed in Claim 4, in which a second gating device is adapted to receive field synchronizing pulses through a controlled switch which switch is closed by a signal when produced by the gate associated with said comparison stage when said compared pulses do not subsist coincidentally, and means for applying an output signal from said second gating device for resetting said frequency divider circuit during the occurrence of said first gating pulse and bringing said bistable element to the state corresponding to that in which said circuit arrangement produces said control signal from said received pulses.

6. A circuit arrangement as claimed in Claim 1, including a free-running oscillator which is adapted to be synchronized either by the divided pulses originating from said frequency divider circuit or by the received field synchronizing pulses to produce said control signals.

7. A circuit arrangement as claimed in Claim 2, in which said gating pulse generator includes an auxiliary frequency divider circuit for dividing the repetition rate of the pulses generated by said frequency divider circuit by the integer *n*.

8. A circuit arrangement as claimed in Claim 7, in which the integer *n* is determined by the condition

$$n \geq \frac{300}{32(N-d)}$$

wherein N is the number of lines per image in a given television standard system and *d* is chosen as a function of the number of lines per image of received television signal of that standard.

9. A circuit arrangement as claimed in any of the preceding Claims, in which the frequency divider circuit, the gating pulse generator, the automatic selection circuit and the gating devices are integrated in a semiconductor body.

10. A circuit arrangement for producing a control signal for the field output stage in a television receiver, substantialy as herein described with reference to the accompanying drawings.

11. A television receiver including a circuit arrangement as claimed in any of the preceding claims.

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