

ABSTRACT

A vertical memory device including gate electrodes on a substrate, the gate electrodes being spaced apart in a first direction and stacked in a staircase arrangement; a channel extending through the gate electrodes in the first direction; a first contact plug extending through a pad of a first gate electrode to contact an upper surface of the first gate electrode, the first contact plug extending through a portion of a second gate electrode, and the second gate electrode being adjacent to the first gate electrode; a first spacer between the first contact plug and sidewalls of the first gate electrode and the second gate electrode facing the first contact plug, the first spacer electrically insulating the first contact plug from the second gate electrode; and a first burying pattern contacting bottom surfaces of the first contact plug and the first spacer, the first burying pattern including an insulating material.

FIG. 46