CLAIMS

1. A complementary metal oxide semiconductor (MOS) (CMOS) standard cell, comprising:
a first supply rail disposed in a direction in a first metal layer;
a second supply rail disposed in the direction in the first metal layer; and
a plurality of metal lines disposed in the direction in the first metal layer, wherein:
each metal line of the plurality of metal lines corresponds to a track of a plurality of tracks;
one or more metal lines of the plurality of metal lines have a cut edge corresponding to a first cell boundary of the CMOS standard cell;
one or more metal lines of the plurality of metal lines have a cut edge corresponding to a second cell boundary of the CMOS standard cell, wherein the second cell boundary is on an opposite side of the CMOS standard cell compared to the first cell boundary; and
one or more metal lines of the plurality of metal lines have an uncut edge corresponding to at least one of the first cell boundary and the second cell boundary.

2. The CMOS standard cell of claim 1, further comprising one or more metal lines disposed in a second metal layer and in a second direction that is substantially orthogonal to the direction.

3. The CMOS standard cell of claim 2, further comprising one or more vertical interconnect accesses (vias) disposed between the first metal layer and the second metal layer, wherein the one or more vias electrically couple one or more metal lines in the second metal layer and one or more metal lines in the first metal layer.

4. The CMOS standard cell of claim 3, wherein:
the first metal layer comprises a metal zero layer (M0);
the second metal layer comprises a metal one layer (M1) disposed above the first metal layer; and
the one or more vias comprise one or more zero level vias (V0).

5. The CMOS standard cell of claim 1, wherein the plurality of metal lines in the first metal layer are disposed between the first supply rail and the second supply rail.

6. The CMOS standard cell of claim 1, wherein:

the first supply rail is disposed between one or more metal lines of the plurality of metal lines in the first metal layer; and

the second supply rail is disposed between one or more metal lines of the plurality of metal lines in the first metal layer.

7. The CMOS standard cell of claim 1 integrated into an integrated circuit (IC).

8. The CMOS standard cell of claim 1 integrated into a device selected from the group consisting of: a set top box; an entertainment unit; a navigation device; a communications device; a fixed location data unit; a mobile location data unit; a global positioning system (GPS) device; a mobile phone; a cellular phone; a smart phone; a session initiation protocol (SIP) phone; a tablet; a phablet; a server; a computer; a portable computer; a mobile computing device; a wearable computing device; a desktop computer; a personal digital assistant (PDA); a monitor; a computer monitor; a television; a tuner; a radio; a satellite radio; a music player; a digital music player; a portable music player; a digital video player; a video player; a digital video disc (DVD) player; a portable digital video player; an automobile; a vehicle component; avionics systems; a drone; and a multicopter.

9. A complementary metal oxide semiconductor (MOS) (CMOS) standard cell circuit, comprising:

a plurality of CMOS standard cells, each CMOS standard cell comprising:

a first supply rail disposed in a direction in a first metal layer;

a second supply rail disposed in the direction in the first metal layer; and

a plurality of metal lines disposed in the direction in the first metal layer, wherein:

each metal line of the plurality of metal lines corresponds to a track of a plurality of tracks;

one or more metal lines of the plurality of metal lines have a cut edge corresponding to a first cell boundary of a corresponding CMOS standard cell;

one or more metal lines of the plurality of metal lines have a cut edge corresponding to a second cell boundary of the corresponding CMOS standard cell, wherein the second cell boundary is on an opposite side of the corresponding CMOS standard cell compared to the first cell boundary; and

one or more metal lines of the plurality of metal lines have an uncut edge corresponding to at least one of the first cell boundary and the second cell boundary;

wherein:

one or more CMOS standard cells of the plurality of CMOS standard cells are disposed such that the second cell boundary of the one or more CMOS standard cells is substantially adjacent to a first cell boundary of one or more other CMOS standard cells; and

one or more metal lines of two or more CMOS standard cells form a single continuous metal line across corresponding tracks of the two or more CMOS standard cells.

10. The CMOS standard cell circuit of claim 9, wherein one or more CMOS standard cells of the plurality of CMOS standard cells further comprise one or more metal lines disposed in a second metal layer and in a second direction that is substantially orthogonal to the direction.

11. The CMOS standard cell circuit of claim 10, wherein one or more CMOS standard cells of the plurality of CMOS standard cells further comprise one or more vertical interconnect accesses (vias) disposed between the first metal layer and the second metal layer, wherein the one or more vias electrically couple one or more metal lines in the second metal layer and one or more metal lines in the first metal layer.

12. The CMOS standard cell circuit of claim 11, wherein:

the first metal layer comprises a metal zero layer (M0);

the second metal layer comprises a metal one layer (M1) disposed above the first metal layer; and

the one or more vias comprise one or more zero level vias (V0).

13. The CMOS standard cell circuit of claim 9, wherein the plurality of metal lines in the first metal layer of each CMOS standard cell are disposed between the first supply rail and the second supply rail.

14. The CMOS standard cell circuit of claim 9, wherein:

the first supply rail of each CMOS standard cell is disposed between one or more metal lines of the plurality of metal lines in the first metal layer; and

the second supply rail of each CMOS standard cell is disposed between one or more metal lines of the plurality of metal lines in the first metal layer.

15. The CMOS standard cell circuit of claim 9, wherein the plurality of CMOS standard cells is arranged to form a buffer.

16. A method for fabricating a CMOS standard cell circuit with dynamically cut metal lines in a first metal layer, comprising:

determining placement of a plurality of metal lines and interconnects disposed above a first metal layer in one or more CMOS standard cells;

determining if a first metal layer layout optimizer is available;

responsive to determining that the first metal layer layout optimizer is available, determining a layout of a plurality of instances of the one or more CMOS standard cells, wherein placement of the plurality of metal lines disposed in the first metal layer in the layout of each instance of the one or more CMOS standard cells is based on an optimized placement of the plurality of metal lines disposed in the first metal layer using orientation and adjacency variables of the one or more CMOS standard cells and a plurality of cell variation templates that define physical attributes of each layout;

responsive to determining that the first metal layer layout optimizer is not available, providing the layout of the plurality of instances of the one or more CMOS standard cells, wherein placement of the plurality of metal lines disposed in the first metal layer in the layout of each instance of the one or more CMOS standard cells corresponds to the placement of the plurality of metal lines disposed in the first metal layer in the plurality of cell variation templates;

for each layout of each instance of the plurality of instances of the one or more CMOS standard cells, determining a plurality of corresponding design costs;

building one or more first metal layer cost-based trees based on one or more corresponding variation seeds, each first metal layer cost-based tree comprising the plurality of design costs corresponding to a combination of the layouts of the one or more CMOS standard cells associated with the corresponding variation seed;

determining the first metal layer cost-based tree that includes the plurality of design costs corresponding to a figure of merit; and

disposing and cutting the plurality of metal lines in the first metal layer according to the layout of each of the one or more CMOS standard cells of the determined first metal layer cost-based tree.

17. The method of claim 16, wherein determining the plurality of corresponding design costs comprises, for each instance of the plurality of instances of the one or more CMOS standard cells, determining a corresponding power cost, performance cost, and area cost.

18. The method of claim 16, further comprising disposing the interconnects and the plurality of metal lines above the first metal layer according to the layout.

19. The method of claim 16, wherein disposing and cutting the plurality of metal lines in the first metal layer comprises:

disposing the plurality of metal lines in the first metal layer; and

cutting one or more metal lines of the plurality of metal lines corresponding to a first cell boundary of a corresponding CMOS standard cell, a second cell boundary of the

corresponding CMOS standard cell, and between the first cell boundary and the second cell boundary of the corresponding CMOS standard cell.

20. The method of claim 16, wherein disposing and cutting the plurality of metal lines comprises disposing and cutting the plurality of metal lines in a metal zero (M0) layer.