Patent Claims

1. A semiconductor wafer composed of monocrystalline silicon having a front side and having a rear side and having a denuded zone, which extends from the front side to the rear side as far as a depth which between a center and an edge of the semiconductor wafer on average is not less than 8 μm and not more than 18 μm, and having a region which adjoins the denuded zone and has BMDs whose density at a distance of 30 μm from the front side is not less than 2×10^9 cm^{-3}.

2. The semiconductor wafer as claimed in claim 1, wherein in the region which adjoins the denuded zone there is a peak density of BMDs which is not less than 4×10^9 cm^{-3}.

3. A method for producing a semiconductor wafer composed of monocrystalline silicon comprising
providing a substrate wafer composed of monocrystalline silicon, which substrate wafer contains interstitial oxygen having a concentration of not less than 4.5×10^{17} atoms/cm^3 und not more than 6.0×10^{17} atoms/cm^3;
an RTA treatment of the substrate wafer, which is subdivided into a first thermal treatment of the substrate wafer at a first temperature in a temperature range of not less than 1160°C and not more than 1190°C for a period of not less than 5 s and not more than 30 s, wherein at least a front side of the substrate wafer is exposed to an atmosphere consisting of argon, and into a second thermal treatment of the substrate wafer at a second temperature in the stated temperature range for a period of not less than 15 s and not more than 35 s, wherein at least the front side of the substrate wafer is exposed to an atmosphere consisting of argon and ammonia.

4. The method as claimed in claim 3, wherein the substrate wafer is heated to the first temperature before the first

thermal treatment at a rate of temperature rise of not less than 50°C/s and not more than 95°C/s and is cooled from the second temperature after the second thermal treatment at a rate of temperature reduction of not less than 25°C/s and not more than 50°C/s.

5. The method as claimed in claim 3 or claim 4, wherein the atmosphere consisting of argon and ammonia has a ratio of argon to ammonia of not less than 10:20 and not more than 10:1.

6. The method as claimed in any of claims 3 to 5, wherein the second thermal treatment is performed within a period of not more than 1 s after the first thermal treatment and the temperature of the substrate wafer between the first and second thermal treatments remains in the temperature range of not less than 1160°C and not more than 1190°C.

7. The method as claimed in any of claims 3 to 6, furthermore comprising performing a double side polishing before the RTA treatment, in the course of which the front side and a rear side of the substrate wafer are polished simultaneously and a material removal of in each case 10 to 30 μm is obtained.

8. The method as claimed in any of claims 3 to 7, furthermore comprising treating the substrate wafer before the RTA treatment with an oxidizing agent in order to obtain on the front side of the substrate wafer a chemically produced oxide layer which is thicker than the thickness of a native oxide layer.

9. The method as claimed in any of claims 3 to 8, furthermore comprising removing a silicon oxynitride layer from the front side of the substrate wafer after the RTA treatment by etching the substrate wafer using an aqueous etchant containing not

less than 0.5% by volume and not more than 1.5% by volume of hydrogen fluoride.

10. The method as claimed in claim 9, furthermore comprising polishing an edge of the substrate wafer before removing the silicon oxynitride layer.

11. The method as claimed in claim 9 or claim 10, furthermore comprising haze-free polishing of the front side of the substrate wafer after the removal of the silicon oxynitride layer, wherein a material removal of not more than 0.5 μm is obtained.

Patent Claims

1. A monocrystalline silicon semiconductor wafer comprising a front side and a rear side, and a denuded zone which extends from the front side to the rear side as far as a depth which, between a center and an edge of the semiconductor wafer, is on average not less than 8 µm and not more than 18 µm, and having a region which adjoins the denuded zone and has BMDs whose density at a distance of 30 µm from the front side is not less than 2×10^{9} cm^{-3}.

2. The semiconductor wafer of claim 1, wherein in the region which adjoins the denuded zone there is a peak density of BMDs which is not less than 4×10^{9} cm^{-3}.

3. A method for producing a monocrystalline silicon semiconductor wafer of claim 1, having a front side and a rear side comprising:

providing a monocrystalline silicon substrate wafer containing interstitial oxygen at a concentration of not less than 4.5×10^{17} atoms/cm^{3} and not more than 6.0×10^{17} atoms/cm^{3};

RTA treating the substrate wafer by a treatment, which comprises a first thermal treatment of the substrate wafer at a first temperature in a temperature range of not less than 1160° C. and not more than 1190° C. for a period of not less than 5 s and not more than 30 s, wherein at least a front side of the substrate wafer is exposed to an atmosphere consisting of argon, and a second thermal treatment of the substrate wafer at a second temperature in the temperature range of not less than 1160° C. and not more than 1190° C. for a period of not less than 15 s and not more than 35 s, wherein at least the front side of the substrate wafer is exposed to an atmosphere consisting of argon and ammonia during said second thermal treatment.

4. The method of claim 3, wherein the substrate wafer is heated to the first temperature before the first thermal treatment at a rate of not less than 50° C./s and not more than 95° C./s and is cooled from the

second temperature after the second thermal treatment at a rate of not less than 25° C./s and not more than 50° C./s.

5. The method of claim 3, wherein the atmosphere consisting of argon and ammonia has a ratio of argon to ammonia of not less than 10:20 and not more than 10:1.

6. The method of claim 4, wherein the atmosphere consisting of argon and ammonia has a ratio of argon to ammonia of not less than 10:20 and not more than 10:1.

7. The method of claim 3, wherein the second thermal treatment is performed within a period of not more than 1 s after the first thermal treatment and the temperature of the substrate wafer between the first and second thermal treatments remains in the temperature range of not less than 1160° C. and not more than 1190° C.

8. The method of claim 4, wherein the second thermal treatment is performed within a period of not more than 1 s after the first thermal treatment and the temperature of the substrate wafer between the first and second thermal treatments remains in the temperature range of not less than 1160° C. and not more than 1190° C.

9. The method of claim 5, wherein the second thermal treatment is performed within a period of not more than 1 s after the first thermal treatment and the temperature of the substrate wafer between the first and second thermal treatments remains in the temperature range of not less than 1160° C. and not more than 1190° C.

10. The method of claim 3, further comprising performing a double side polishing before the RTA treatment, in the course of which the front side and the rear side of the substrate wafer are polished simultaneously and a material removal of 10 to 30 µm is obtained on each side.

11. The method of claim 3, further comprising treating the substrate wafer before the RTA treatment with an oxidizing agent in order to obtain on the front side of the substrate wafer a chemically produced oxide layer which is thicker than the thickness of a native oxide layer.

12. The method of claim 4, further comprising treating the substrate wafer before the RTA treatment with an oxidizing agent in order to obtain on the front side of the substrate wafer a chemically produced oxide layer which is thicker than the thickness of a native oxide layer.

13. The method of claim 5, further comprising treating the substrate wafer before the RTA treatment with an oxidizing agent in order to obtain on the front side of the substrate wafer a chemically produced oxide layer which is thicker than the thickness of a native oxide layer.

14. The method of claim 7, further comprising treating the substrate wafer before the RTA treatment with an oxidizing agent in order to obtain on the front side of the substrate wafer a chemically produced oxide layer which is thicker than the thickness of a native oxide layer.

15. The method of claim 3, further comprising removing a silicon oxynitride layer from the front side of the substrate wafer after the RTA treatment by etching the substrate wafer using an aqueous etchant containing not less than 0.5% by volume and not more than 1.5% by volume of hydrogen fluoride.

16. The method of claim 4, further comprising removing a silicon oxynitride layer from the front side of the substrate wafer after the RTA treatment by etching the substrate wafer using an aqueous etchant containing not less than 0.5% by volume and not more than 1.5% by volume of hydrogen fluoride.

17. The method of claim 5, further comprising removing a silicon oxynitride layer from the front side of the substrate wafer after the RTA treatment by etching the substrate wafer using an aqueous etchant containing not less than 0.5% by volume and not more than 1.5% by volume of hydrogen fluoride.

18. The method of claim 7, further comprising removing a silicon oxynitride layer from the front side of the substrate wafer after the RTA treatment by etching the substrate wafer using an aqueous etchant containing not less than 0.5% by volume and not more than 1.5% by volume of hydrogen fluoride.

19. The method of claim 15, further comprising polishing an edge of the substrate wafer before removing the silicon oxynitride layer.

20. The method of claim 9, further comprising haze-free polishing the front side of the substrate wafer after the removal of the silicon oxynitride layer, wherein a material removal of not more than 0.5 µm is obtained.