Descripti

Field of the Invention

This invention relates to video signal processors for progressive scan video systems of the type that convert line-rate interlaced video signals into double line-rate non-interlaced video signals and wherein added lines are obtained by interpolation.

Background of the Invention

"Progressively" scanned television receivers have been proposed wherein the horizontal scan rate is multiplied, i.e., doubled, and each line of video is displayed twice thereby providing a displayed image having reduced visibility of line structure and subjectively improved vertical resolution. In a typical progressively scanned receiver, each line of video is stored in one of two memories. As a first of the memories is being written with the incoming video signal at a standard line rate, the second of the memories is read times at twice the standard line rate thereby providing two lines of "speed-up" (time-compressed) video within one standard line interval. The second memory output is applied to a display having a doubled horizontal sweep rate synchronized with read-out of the memory thereby doubling the number of displayed lines of video signal. An example of such a progressively scanned receiver, wherein the added lines of video signal are replicas of the original scan lines, is described in U. S. Patent US-A-4,415,931 entitled TELEVISION DISPLAY WITH DOUBLED HORIZONTAL LINES which issued November 15, 1983 to R. A. Dischert.

It has been recognized that a desirable reduction of certain artifacts (e.g., inter-line flicker, line break-up with motion, etc.) may be obtained in a progressively scanned receiver by interpolating the added lines of the video signal from the original signal. This may be done either before or after "speed-up" (i.e., time compressing) of the video signal in the memory. An example of a progressively scanned display system in which the additional scan lines are obtained by interpolation from the original scanlines prior to time compression or video "speed-up" is described by K. H. Powers in U.S. Patent US-A-4,400,719 entitled TELEVISION DISPLAY SYSTEM WITH REDUCED LINE SCAN ARTIFACTS which issued August 23, 1983. An alternative of providing interpolation subsequent to speed-up of the video signal is described by Yasushi Fujimura et al. in UK Patent Application GB-A-2,111,343A according to which successive lines of the video signal are successively read into two memories at one clock rate and are successively read out at a speeded up clock rate into an interpolator (in this case an averaging interpolator) by which interpolated speeded up lines are derived from successive pairs of time-adjacent lines as read out from the memories. In all of these interpolating progressive scan receivers, separate clocked memories or delays (e.g., a CCD or a RAM) are connected in cascade for providing the interpolation and speed-up functions.

It is herein recognized that the use of separate clocked memories in cascade for providing the functions of interpolation and time compression can result in a requirement for meeting very critical clock timing requirements. This problem arises because where memories are cascaded, the first memory in the cascade connection must "settle" before the information recovered from it can be written into the second memory and the settling time may comprise a significant portion of a clock cycle. The read clock in an NTSC processor, for example, typically operates at a frequency of about 28 MHz (i.e., eight times the color subcarrier frequency, $8f_{sc}$) and thus has a period of only about 36 nano-seconds. To meet this timing requirement, and to allow a reasonable margin for manufacturing tolerances, it may be necessary to resort to the use of multiphase clocks or to use special clock delay lines to properly time the operation of separate interpolator and time compressor memories.

The present invention is directed to meeting the need for an interpolating progressive scan video signal processor in which the aforementioned clock timing problems are substantially reduced. In accordance with the present invention as claimed in claim 1, a processor includes parallel arranged common memories for providing the functions of interpolation and time compression of a video signal being processed.

Brief Description of the Drawing

The invention is illustrated in the accompanying drawing, wherein like elements are denoted by like reference designators, and in which:

FIGURE 1 is a block diagram of a television receiver having a processor embodying the invention;

FIGURE 2 is a detailed block diagram of a timing signal generator and switching arrangement suitable for use in the receiver of FIGURE 1;

FIGURE 3 is a timing diagram associated with FIGURES 1 and 2;

FIGURE 4 is a block diagram illustrating a modification of the processor shown in Figure 1;

FIGURE 5 illustrates a modification of FIGURE 2;

and

FIGURE 6 is a timing diagram associated with FIGURES 4 and 5.

Detailed Description

The principles of the invention may be applied to the processing of component video signals such as Y, I, Q or R, G, B. In the specific example of FIGURE 1, the video processor 10 (outlined in phantom) embodying the invention is used for providing interpolation and time compression of the luminance component, Y, of a video signal in an interpolating progressively scanned television receiver. The receiver includes an antenna terminal 12 coupled to a tuner/I.F./detector unit 14 of conventional design which processes RF input

signals supplied to terminal 12 from a source (e.g., an antenna, tape recorder, disc player or the like) to provide a baseband composite video output signal S1. For purposes of illustration, it will be assumed that signal S1 is an NTSC standard interlaced signal having 525 lines per frame, two fields per frame, a field rate of about 60 fields per second, a line rate of about 15 KHz and a color subcarrier frequency of about 3.58 MHz. It will be appreciated, of course, that the principles of the invention apply also to other video signal formats (e.g., PA multiplexed analog component type system, etc.).

The composite video signal S1 is applied to a synchronizing signal detector 16 which supplies horizontal (HS) and vertical (VS) synchronizing signals to the yoke of a kinescope 18 via horizontal and vertical drive units 20 and 22, respectively. The horizontal synchronizing signal HS is doubled in frequency by means of a frequency doubler 24 prior to being applied to drive unit 20 to thereby double the horizontal scan rate of kinescope 18. The field rate (60/sec) is unchanged whereby a raster is produced on kinescope 18 having 525 lines per field.

Signal S1 is also applied to a luminance/chrominance (Y/C) separator 26 (e.g., a comb filter) which separates the luminance and chrominance components and supplies the chrominance component C to a chroma processor 28 which provides the functions of line doubling and demodulation of the chroma signal and produces double line rate color difference signals R-Y and B-Y. The line doubling of the chroma signal could be performed by a processor similar to processor 10 if interpolation were desired. Chroma interpolation, however, is not necessary as a satisfactory color image may be obtained by merely repeating each line of chroma without any interpolation.

The luminance signal Y provided by separator 26 is applied to processor 10 which doubles the number of lines per field by inserting an additional line (obtained by interpolation) between each pair of received lines. The processed video signal Y' produced by processor 10 is at the double line rate and applied along with the double line rate color difference signals R-Y and B-Y provided by processor 28 to a matrix 30 which generates R, G and B drive signals for kinescope 18. The displayed image on kinescope thus comprises 525 lines per field with the added lines of chroma being replicas of the received lines (no interpolation) and the added lines of luma being interpolated versions of the received lines.

Processor 10, embodying the invention, includes a parallel type of arrangement of three one-line (1-H) clocked memories 32, 34 and 36. Illustratively, the memories may be either of the charge coupled device (CCD) type or the random access memory (RAM) type, both being well known. In this example of the invention, it will be assumed that memories 32, 34 and 36 are each RAM type devices.

The incoming or "received" luminance signal Y is converted to digital form (YD) for storage in memories 32, 34 and 36 by means of an A/D converter 40. Signal YD is sequentially applied to memories 32, 34 and 36 by means of a three position input switch 50 which is "stepped" or sequenced at the incoming line rate. For example, during the first line of a field, YD is coupled to memory 32. During the second and third lines, signal YD is coupled to memories 34 and 36, respectively. The sequence then repeats with signal YD being applied to memory 32 during the fourth line.

Read and write clock signals (FR and FW, respectively) for memories 32-36 are provided by a timing signal generator 42 which, as will be explained in connection with FIGURE 2, also provides timed signals for operating switch 50, a clock switch 52 and an output switch 54 in processor 10. The read clock frequency FR is selected to be twice the write clock frequency FW. It is also convenient that the FR and FW be multiples of the color subcarrier frequency FSC to facilitate clock signal generation by relatively simple phase locked loops which produce signals locked frequency and phase to the color burst. Illustrative values are 4 FSC for FW or about 14 MHz (for NTSC signals) and 8 FSC or about 28 MHz for FR.

The read and write clock signals FR and FW are applied to memories 32-36 by means of a clock switch 52 that is operated synchronously with the input switch 50 under control of unit 42 as follows. When switch 50 applies the digitized luma signal YD to one of the memories 32-36, switch 52 applies the write clock FW signal to the clock input (CL) of the selected memory and simultaneously applies the read clock signal FR to the clock inputs of the remaining two memories. As a result, during the time interval that one memory is in the process of writing in a current line of the luma signal YD, the other two memories are reading out previously stored lines of the luma signal YD twice. This follows since the read clock frequency is exactly twice the write clock frequency. For the switch positions shown, memory 32 is coupled to receive the luma signal YD and the write clock signal FR while memories 34 and 36 are each coupled to receive the read clock signal FR. After the current line of luma is stored in memory 32, switch 50 is stepped to store the next line of luma in memory 34 and switch 52 is changed over to apply the write clock signal FW to memory 34 and to apply the read clock signal FR to memories 32 and 36. This cycle continues line by line throughout the field with two memories containing the two previously stored video signals being read while one memory is writing the currently received line.

The described parallel type organization of three memories which concurrently reads two previously stored lines while writing the current line is a significant feature of this invention. This organization facilitates generation of interpolated lines concurrently with the speed-up memory read/write operation using the same memory

elements that provide video line doubling and significantly reduces the potential for timing errors to occur which is inherent in the previously discussed prior art systems which have memories organized in cascade or serial fashion and which provide interpolation prior to or after video speed-up.

Interpolation is performed by averaging the outputs of each pair of the three memories. This is done by connecting adders 60, 62 and 64 to the outputs of each pair of memories 32-34, 34-36 and 36-32, respectively. This provides the sum of each pair of lines. The average is obtained by dividing the sum by two in dividers 66, 68 and 70 connected to the respective outputs of adders 60, 62 and 64. In the case where memories 32-36 are CCD devices rather than RAM devices, the addition (summing) and division (attenuating by 6db) may be provided by simple resistor networks.

The processed luminance signal Y' is obtained by means of an output switch 54 which sequentially selects one of the outputs of memories 32-and dividers 66-70 and applies the selected output to matrix 30 via a digital-to-analog converter 72. Switch 54 is controlled by timing signal generator 42 to advance (step) at twice the rate of switch 50. The phasing of switch 54 with respect to switch 50 is such that switch 54 "reads" the output of one of the memories and then reads the interpolated output of two of the memories during the time period that the third memory is being written.

Illustratively, for the switch position shown, switch 54 sequentially selects the outputs of memory 34 and divider 68 during the time that memory 32 is being written. When switch 50 advances one step to store the next incoming line in memory 34, switch 54 then advances to sequentially "read" the outputs of memory 36 and adder 70. The overall result is a sequence of lines is displayed on kinescope 18 that alternates between "real" lines provided by memories 32-36 and interpolated lines provided by dividers 66-70. The incoming lines are denoted by A, B, C and D, then the output line sequence will be A, (A+B)/2, B, (B+C)/2, C,(C+D)/2, D and so on.

FIGURE 2 is examplary of a suitable implementation of timing signal generator 42 and switches 50, 52 and 54. For clarity in the drawing, video signal buses are represented as single lines as was done in FIGURE 1. Also, gates coupled to video lines are shown as single gates although in practice they would actually be parallel gates equal in number to the number of bus conductors.

Timing for operating all switches and generating memory write enable signals is provided by a modulo six (6) counter 202 which is clocked by the double line rate horizontal sync signal 2HS provided by sync detector 16. The output of counter 202 comprises a 3 bit binary word having six possible states. The counter advances one count for each horizontal line scan of kinescope 18. Two counts thus correspond to one line scan interval of the incoming video signal and one count corresponds to one line scan interval of the "speed-up" or processed video output signal.

The count is decoded in a one-of-six (1 of 6) decoder 204 to thereby provide enabling outputs for six AND gates 206-211 which comprises output switch 54. Assuming that the video signal comprises 8 bits, each gate would be implemented as 8 parallel gates as previously noted. When using CCD type memories, gates 206-211 may be transmission gates. Note that the decoded outputs of decoder 204 are connected to gates 206-211 such that gate 208 is enabled during the interval that the count is zero ("0") thereby coupling the output of memory 34 to D/A converter 72. This corresponds to the condition of switch 54 shown graphically in FIGURE 1. As the count progresses, gates 208-211 and 206-207 are sequentially enabled as shown in FIGURE 3 where an enabled condition is signified by a high level of the waveform.

The decoded outputs of decoder 204 are additionally decoded by three OR gates 220, 224 and 226 to generate write enable for memories 32, 34 and 26 and control signals for input switch 50 at the incoming line rate. Switch 50 comprises three AND gates 230, 232 and 234. Gate 220 is enabled by the "0" and "1" outputs of decoder 204 and provides the write enable signal for memory 36 and an enable signal for gate 230. Gate 222 is enabled by the "2" and "3" outputs of decoder 204 and provides the write enable signal for memory 34 and the enable signal for gate 232 of switch 50. Gate 224 is enabled by the "4" and "5" outputs of decoder 204 and provides the write enable signal for memory 36 and enable signal for gate 234. The described sequence of enablement of gates 224-234 and generation of write enable signals is illustrated in FIGURE 3.

The remaining elements of FIGURE 2 illustrate how the read (FR) and write (FR) clock signals for memories 32-36 may be generated and how the clock switch 52 may be constructed. The read clock signal, FR, is provided by means of a multiplying phase locked loop 240 which receives the composite video signal SI and locks an oscillator to eight times the frequency of the color burst component of signal SI. The write clock signal, FW, is produced by dividing signal FR by two in a divider 242. Switch 52 comprises three selection gates each comprised of a pair of AND and one OR gates. Signal FR is applied to one AND gate (251, 261, 271) of each selection gate and signal FW is applied to the other AND gate (250, 260, 270) of each selection gate. The outputs of each AND gate of each pair in a selection gate are applied to an OR gate to generate the memory clock signals. Specifically, gates 250 and 251 are coupled to gate 252, gates 260 and 261 are coupled to gate 262 and gates 270 and 271 are coupled to gate 272. The circles at the inputs of gates 251, 261 and 271 signify negative true logic. That is, the gate is enabled when the circled input is low. This is merely a shorthand way of signifying the presence of an inverter at the circled input.

Gates 250 and 251 are controlled by gate 220

such that during counts "0" and "1" gate 250 is enabled and gate 251 is disabled thereby applying the write clock FR to memory 32 during this time interval. At all other times gate 251 is enabled (gate 220 low) thereby applying the read clock to memory 32. The remaining gates are similarly controlled during subsequent lines (i.e., time intervals corresponding to counts "2", "3" and counts "4", "5").

Overall operation of processor 10 during four lines of the video input signal Y is summarized in FIGURE 3. For illustrative purposes, the count of counter 201 is assumed to be zero at the beginning of line 4 of the video input signal, Y. As shown in the memory 32-36 timing diagram, memory 32 writes in line 4 as it is received, reads out the stored line four times during lines 5 and 6 and then stores line 7. As memory 32 is being written with line 4, memory 34 reads at the previously stored line 2 twice, writes in line 5 and then reads out line 5 four times as lines 6 and 7 are received. Memory 36 reads out a previously stored line 3 four times during the time lines 4 and 5 are received, writes in line 6 and then begins reading out line 6.

As shown in the output switch selection diagram, switch 54 selects the output of memory 34 when the count is zero. Thus, during the first half of incoming line 4, the video output signal corresponds to line 2 from memory 34. Since the read clock frequency is double that of the write clock, the recovered line 2 is "speeded-up" or "compressed" by a factor of two with respect to the incoming line rate. During count 1 switch 54 selects the output of divider 68 which contains the average of the lines stored in memories 34 and 36, namely, one half of the sum of lines 2 and 3. As switch 54 advances, the video output signal alternates between the compressed received lines and the compressed interpolated lines to form the output sequence shown in the "video out" diagram.

FIGURE 4 illustrates a desirable modification of processor 10 which has substantially simplified output signal forming circuitry with a reduced number of adders and dividers. In this case. timed switching effects coupling of both averaging circuit inputs to the output of one memory during one line interval of consecutive lines intervals, and both inputs of the averaging circuit to the outputs of separate memories during the next line. This provides an output signal from the averaging circuit in which non-interpolated time-compressed lines of video obtained from one of two memories being read are interleaved with interpolated time-compressed lines of video obtained by averaging the output signals of two of the memories being read. In this modification, the adders 60-64, divider 66-70 and switch 54 of FIGURE 1 are replaced by a single adder 82, a single divider 84 and two switches 54A and 54B in Figure 4. Generator 42 is also modified as will be explained. Switches 54A and 54B each have three inputs connected to respective ones of the outputs of memories 32.34 and 36. The outputs of switches 54A and 54B are connected to the inputs of adder 82 which has an output coupled via divider 84 to the input of D/A converter 72. For any position of switches 54A and 54B. adder 82 and divider 84 average the switch output signals (i.e., sum and divide by two). As a first example, if switch 54A is coupled to receive line "X" from one memory and switch 54B is coupled to received line "Y" from a different memory, then the divider 84 output is an interpolated or averaged line (X+Y)/2. If, however, both switches are coupled to the same memory containing, say, line X, then the output is (X+X)/2 or simply X. Thus, even though all output signals pass through adder 82 and divider 84, these elements function as a two-point interpolator if the input signals differ, and function as a "conduit", so to speak, if the input signals are the same.

In operation, the input switch 50 and clock switch 52 function as previously described to sequentially write the incoming video signal (YD, in this case) into memories 32-36. Switches 54A and 54B couple adder 82 to the memories in the sequence shown in FIGURE 6 by the timing diagrams labeled "switch 54A" and "switch 54B". During count "0" (the first half of line 4) switches 54A and B couple both inputs of adder 82 to the output of memory 34 to receive line 2 previously stored therein. Since the "average" of line 2 is line 2, the video output during count "0" is line 2. During count "1", the inputs of adder 82 are coupled to the output of memories 34 and 36 to receive lines 2 and 3, respectively. The video output is thus a two-point interpolation or average of these lines, namely, (line 2 + line 3)/2 as indicated. This process repeats, as shown, so that the resultant video output signal alternates between speeded-up (compressed) "real" (received) lines and "interpolated" lines as shown. This is the same sequence as in FIGURE 3 but fewer adders and dividers are required thereby reducing the cost and improving the reliability (by parts count reduction) of the processor.

FIGURE 5 illustrates how FIGURE 2 may be modified to implement switches 54A and 54B and to generate appropriate switch timing signals. The timing signals are generated by means of six OR gates 501-506 coupled to the outputs of decoder 204 as shown. Switch 54A comprises three AND gates 510-512 coupled to an OR gate 520. Switch 54B comprises three AND gates 513-515 coupled to an OR gate 530. Each gate, as previously explained, may actually comprise a number of parallel gates equal to the number of conductors of the video bus.

Gates 510, 511 and 512 couple the outputs of memories 32, 34 and 36, respectively, to adder 82 via OR gate 520 when enabled by OR gates 501, 502 and 503, respectively. Gates 513, 514 and 515 couple the output of memories 32, 34 and 36 to the other input of adder 82 via OR gate 530 when enable by OR gates 504, 505 and 506, respectively. Gates 501-506 are coupled to the decoder 204 outputs to enable gates 510-515 in accord-

ance with the switch timing indicated in FIGURE 6. As an example, gates 502 and 505 enable gates 511 and 514. respectively, when the count is "0" thereby coupling both inputs of adder 82 to the output of memory 34 to thus provide a non-interpolated line "2" video output signal. During count "1" gates 503 and 505 enable gates 512 and 514 thereby coupling the outputs of memories 36 and 34 to adder 82 to provide the interpolated line (2+3)/2 video output signal. The remaining gates are similarly connected, as shown, to provide the switch sequence shown and previously discussed in connection with FIGURE 6.

Claims

1. A progressive scan processor comprising a source of video input signal and a plurality of memories which cooperate to provide an output video signal in which alternate video lines have been interpolated from adjacent lines, characterized in that three line memories (32, 34, 36), each having a storage capacity of one line of said video input signal, are associated with memory control means (50, 42) for causing current lines of said video signal to be written successively into respective ones of said three memories, a line at a time, at a first clock rate (FW) and, while said video signal is being written into one of said memories, for causing two previously stored lines to be read from the other two of said memories at a second clock rate (FR) to provide a pair of time-compressed video signals; and with means (54, 60-70) coupled to said memories and responsive to such pairs of time-compressed video signals for providing by interpolation therefrom said alternate lines of said video output signal (Y').

2. A processor as recited in claim 1 wherein said output means includes averaging circuitry (60, 66; 62, 68:64, 70) for forming an average of said two time-compressed video signals provided by each pair (32, 34; 34, 36; 36, 32) of said memories, and applying to an output terminal, a line at a time, averaged time-compressed video signals alternating with non-interpolated time-compressed video signals derived from the memories.

3. A processor as recited in claim 1 wherein said output means includes at least one averaging circuit (60, 66) and at least one switch (54) coupled to said memories for forming a processed video output signal in which non-inter-polated time-compressed lines derived from said memories alternate with lines which are time-compressed and formed by averaging.

4. A processor as recited in claim 2 or 3 wherein said output means includes a separate averaging circuit (60/66; 62/68; 64/70) for each pair (32/34; 34/36; 36/32) of said three memories.

5. A processor as recited in claim 3 wherein said output means comprises three averaging circuits (60/66;62/68;64/70) connected between respective pairs (32/34;34/36;36/32) of said memories and wherein said switch (54) has three inputs coupled to respective ones of said memories (32,34,36), three further inputs coupled to respective ones of said averaging circuits and an output at which it provides said processed video output signal with alternate lines thereof consisting of non-interpolated time-compressed lines derived from said memories and with intermediate lines thereof consisting of time compressed and averaged lines obtained from said averaging circuits.

6. A processor as recited in claim 1 wherein said output means includes solely one averaging circuit (82/84) having first and second inputs and, coupled to said inputs, respective switches (54A, 54B)) operable to selectively couple said inputs to outputs of said memories for forming said processed video output signal with alternate lines thereof consisting of non-interpolated time-compressed lines and with intermediate lines consisting of time-compressed and averaged lines obtained from said averaging circuit.

7. A processor as recited in claim 6 including switch control means for controlling said switches to selectively couple both inputs of said averaging circuit to one of the two memories which are being read during a first time interval, and for coupling said inputs of said averaging circuit to respective ones of the two memories which are being read during a second time interval, to provide said video output signal from the averaging circuit as a combination of non-interpolated time-compressed lines each obtained from one memory and, interleaved therewith, averaged timecompressed lines each obtained from two memories.

8. A processor as recited in claim 7 wherein each of said switches (54A, 54B) has three inputs, each input being connected to a respective one of said memories (32, 34, 36), and an output connected to the respective input of said averaging circuit (82/84); and said switch control means includes a timing signal generator (Fig. 5) for controlling said switches to couple one of said two time-compressed video signals to both inputs of said signal averaging circuit during a first time interval and for coupling said two time-compressed video signals to respective ones of said inputs of said averaging circuit during a second time interval.

Patentansprüche

1. Verarbeitungseinrichtung für Zeilenfolgeabtastung, mit einer Quelle eines Videoeingangssignals und einer Vielzahl von Speichern, die zusammenwirken, um ein Videoausgangssignal zu liefern, in welchem ein über die andere abwechselnde Videozeilen aus benachbarten Zeilen interpoliert worden sind, dadurch gekennzeichnet, daß drei Zeilenspeicher (32, 34, 36), deren jeder eine Speicherkapazität von einer Zeile des besagten Videoeingangssignals hat, einer Speichersteuereinrichtung (50, 42) zugeordnet sind, um zu bewirken, daß laufende Zeilen des besagten Videosignals nacheinander mit einer

ance with the switch timing indicated in FIGURE 6. As an example, gates 502 and 505 enable gates 511 and 514. respectively, when the count is "0" thereby coupling both inputs of adder 82 to the output of memory 34 to thus provide a non-interpolated line "2" video output signal. During count "1" gates 503 and 505 enable gates 512 and 514 thereby coupling the outputs of memories 36 and 34 to adder 82 to provide the interpolated line (2+3)/2 video output signal. The remaining gates are similarly connected, as shown, to provide the switch sequence shown and previously discussed in connection with FIGURE 6.

Claims

1. A progressive scan processor comprising a source of video input signal and a plurality of memories which cooperate to provide an output video signal in which alternate video lines have been interpolated from adjacent lines, characterized in that three line memories (32, 34, 36), each having a storage capacity of one line of said video input signal, are associated with memory control means (50, 42) for causing current lines of said video signal to be written successively into respective ones of said three memories, a line at a time, at a first clock rate (FW) and, while said video signal is being written into one of said memories, for causing two previously stored lines to be read from the other two of said memories at a second clock rate (FR) to provide a pair of time-compressed video signals; and with means (54, 60-70) coupled to said memories and responsive to such pairs of time-compressed video signals for providing by interpolation therefrom said alternate lines of said video output signal (Y').

2. A processor as recited in claim 1 wherein said output means includes averaging circuitry (60, 66; 62, 68:64, 70) for forming an average of said two time-compressed video signals provided by each pair (32, 34; 34, 36; 36, 32) of said memories, and applying to an output terminal, a line at a time, said averaged time-compressed video signals alternating with non-interpolated time-compressed video signals derived from the memories.

3. A processor as recited in claim 1 wherein said output means includes at least one averaging circuit (60, 66) and at least one switch (54) coupled to said memories for forming a processed video output signal in which non-inter-polated time-compressed lines derived from said memories alternate with lines which are time-compressed and formed by averaging.

4. A processor as recited in claim 2 or 3 wherein said output means includes a separate averaging circuit (60/66; 62/68; 64/70) for each pair (32/34; 34/36; 36/32) of said three memories.

5. A processor as recited in claim 3 wherein said output means comprises three averaging circuits (60/66;62/68;64/70) connected between respective pairs (32/34;34/36;36/32) of said memories and wherein said switch (54) has three inputs coupled to respective ones of said memories (32,34,36), three further inputs coupled to respective ones of said averaging circuits and an output at which it provides said processed video output signal with alternate lines thereof consisting of non-interpolated time-compressed lines derived from said memories and with intermediate lines thereof consisting of time compressed and averaged lines obtained from said averaging circuits.

6. A processor as recited in claim 1 wherein said output means includes solely one averaging circuit (82/84) having first and second inputs and, coupled to said inputs, respective switches (54A, 54B)) operable to selectively couple said inputs to outputs of said memories for forming said processed video output signal with alternate lines thereof consisting of non-interpolated time-compressed lines and with intermediate lines consisting of time-compressed and averaged lines obtained from said averaging circuit.

7. A processor as recited in claim 6 including switch control means for controlling said switches to selectively couple both inputs of said averaging circuit to one of the two memories which are being read during a first time interval, and for coupling said inputs of said averaging circuit to respective ones of the two memories which are being read during a second time interval, to provide said video output signal from the averaging circuit as a combination of non-interpolated time-compressed lines each obtained from one memory and, interleaved therewith, averaged timecompressed lines each obtained from two memories.

8. A processor as recited in claim 7 wherein each of said switches (54A, 54B) has three inputs, each input being connected to a respective one of said memories (32, 34, 36), and an output connected to the respective input of said averaging circuit (82/84); and said switch control means includes a timing signal generator (Fig. 5) for controlling said switches to couple one of said two time-compressed video signals to both inputs of said signal averaging circuit during a first time interval and for coupling said two time-compressed video signals to respective ones of said inputs of said averaging circuit during a second time interval.

Patentansprüche

1. Verarbeitungseinrichtung für Zeilenfolgeabtastung, mit einer Quelle eines Videoeingangssignals und einer Vielzahl von Speichern, die zusammenwirken, um ein Videoausgangssignal zu liefern, in welchem ein über die andere abwechselnde Videozeilen aus benachbarten Zeilen interpoliert worden sind, dadurch gekennzeichnet, daß drei Zeilenspeicher (32, 34, 36), deren jeder eine Speicherkapazität von einer Zeile des besagten Videoeingangssignals hat, einer Speichersteuereinrichtung (50, 42) zugeordnet sind, um zu bewirken, daß laufende Zeilen des besagten Videosignals nacheinander mit einer

ersten Taktfrequenz (FW) in jeweilige Exemplare der drei Speicher eingeschrieben werden, jeweils eine Zeile auf einmal, und um während des Einschreibens des besagten Videosignals in jeweils einen der besagten Speicher zu bewirken, daß zwei vorher gespeicherte Zeilen aus den anderen beiden Speichern mit einer zweiten Taktfrequenz (FR) ausgelesen und dadurch ein Paar zeitlich komprimierter Videosignale geliefert werden; und mit einer Einrichtung (54, 60-70), die mit den besagten Speichern gekoppelt ist und auf solche Paare zeitlich komprimierter Videosignale anspricht, um daraus durch Interpolation die besagten abwechselnden Zeilen des Videoausgangssignals (Y') zu liefern.

2. Verarbeitungseinrichtung nach Anspruch 1, worin die besagte Ausgangseinrichtung eine mittelwertbildende Schaltungsanordnung (60, 66; 62, 68: 64, 70) enthält, um einen Mittelwert der beiden von jedem Paar (32, 34; 34, 36; 36, 32) der besagten Speicher gelieferten zeitlich komprimierten Videosignale zu bilden und um die gemittelten zeitlich komprimierten Videosignale, jeweils eine Zeile auf einmal, abwechselnd mit von den Speichern abgeleiteten nichtinterpolierten zeitlich komprimierten Videosignalen an eine Ausgangsklemme zu legen.

3. Verarbeitungseinrichtung nach Anspruch 1, worin die besagte Ausgangseinrichtung mindestens eine Mittelungsschaltung (60, 66) und mindestens einen Schalter (54) enthält, gekoppelt mit den besagten Speichern, um ein verarbeitetes Videoausgangssignal zu bilden, in welchem aus den Speichern abgeleitete nicht-interpolierte zeitlich komprimierte Zeilen mit Zeilen abwechseln, die zeitlich komprimiert und durch Mittelung gebildet sind.

4. Verarbeitungseinrichtung nach Anspruch 2 oder 3, worin die besagte Ausgangseinrichtung für jedes Paar (32/34; 34/36; 36/32) der besagten drei Speicher eine gesonderte Mittelungsschaltung (60/66; 62/68; 64/70) enthält.

5. Verarbeitungseinrichtung nach Anspruch 3, worin die besagte Ausgangseinrichtung drei Mittelungsschaltungen (60/66; 62/68; 64/70) aufweist, die zwischen jeweilige Paare (32/34; 34/36; 36/32) der besagten Speicher geschaltet sind, und worin der besagte Schalter (54) drei Eingänge hat, die mit jeweiligen Exemplaren der besagten Speicher (32, 34, 36) gekoppelt sind, und drei weitere Eingänge, die mit jeweiligen Exemplaren der Mittelungsschaltungen gekoppelt sind, und einen Ausgang, an dem er das besagte verarbeitete Videoausgangssignal liefert, in welchem abwechselnde Zeilen aus von den besagten Speichern abgeleiteten nicht-interpolierten zeitlich komprimierten Zeilen bestehen und dazwischenliegende Zeilen aus von den besagten Mittelungsschaltungen erhaltenen zeitlich komprimierten und gemittelten Zeilen bestehen.

6. Verarbeitungseinrichtung nach Anspruch 1, worin die besagte Ausgangseinrichtung nur eine Mittelungsschaltung ((82/84) mit einem ersten und einem zweiten Eingang enthält und mit den besagten Eingängen jeweils verbundene Schalter (54A, 54B) enthält, die betreibbar sind, um die besagten Eingänge selektiv mit Ausgängen der besagten Speicher zu koppeln und dadurch das verarbeitete Videoausgangssignal zu bilden, bei welchem abwechselnde Zeilen aus nicht-interpolierten zeitlich komprimierten Zeilen bestehen und dazwischenliegende Zeilen aus zeitlich komprimierten und von der Mittelungsschaltung erhaltenen gemittelten Zeilen bestehen.

7. Verarbeitungseinrichtung nach Anspruch 6, enthaltend eine Schaltersteuereinrichtung zur Steuerung der besagten Schalter, um selektiv beide Eingänge der besagten Mittelungsschaltung während eines ersten Zeitintervalls mit einem der beiden gerade ausgelesenen Speicher zu koppeln und um die besagten Eingänge der besagten Mittelungsschaltung während eines zweiten Zeitintervalls mit jeweils einem gesonderten Exemplar der beiden gerade ausgelesenen Speicher zu koppeln, um das besagte Videoausgangssignal von der Mittelungsschaltung zu liefern als eine Kombination aus nicht-interpolierten zeitlich komprimierten Zeilen, deren jede aus einem Speicher erhalten wird, und, verschachtelt damit, gemittelte zeitlich komprimierte Zeilen, deren jede aus zwei Speichern erhalten wird.

8. Verarbeitungseinrichtung nach Anspruch 7, worin jeder der besagten Schalter (54A, 54B) drei Eingänge hat, deren jeder mit einem jeweiligen Exemplar der besagten Speicher (32, 34, 36) verbunden ist, und einen Ausgang, der mit dem jeweiligen Eingang der Mittelungsschaltung (82/84) verbunden ist; und die besagte Schaltersteuereinrichtung einen Zeitsignalgenerator (Fig. 5) enthält, um die besagten Schalter so zu steuern, daß während eines ersten Zeitintervalls eines der besagten beiden zeitlich komprimierten Videosignale auf beide Eingänge der besagten Signalmittelungsschaltung gekoppelt wird und daß während eines zweiten Zeitintervalls die besagten beiden zeitlich komprimierten Videosignale auf jeweils zugeordnete Exemplare der besagten Eingänge der besagten Mittelungsschaltung gekoppelt werden.

Revendications

1. Processeur à balayage progressif comprenant une source d'un signal vidéo d'entrée et un certain nombre de mémoires qui coopèrent pour produire un signal vidéo de sortie, où des lignes vidéo alternées ont été interpolées à partir de lignes adjacentes, caractérisé en ce que trois mémoires de ligne (32, 34, 36), chacune ayant une capacité de stockage d'une ligne dudit signal d'entrée vidéo, sont associées à des moyens de commande de mémoire (50, 42) pour forcer les lignes courantes dudit signal vidéo à être inscrites en succession dans des mémoires respectives desdites trois mémoires, une ligne à la fois, à une première fréquence d'horloge (FW) et, tandis que ledit signal vidéo est inscrit dans l'une desdites mémoires, pour forcer deux lignes précédemment stockées à être lues des deux autres des-

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dites mémoires à une seconde fréquence d'horloge (FR) pour produire une paire de signaux vidéo comprimés dans le temps; et avec un moyen (54, 60-70) couplé auxdites mémoires et répondant auxdites paires de signaux vidéo comprimés dans le temps pour produire, par interpolation, lesdites lignes alternées dudit signal vidéo de sortie (Y').

2. Processeur selon la revendication 1, où ledit moyen de sortie comprend un montage faisant la moyenne (60, 66; 62, 68:64, 70) pour former une moyenne desdits deux signaux vidéo comprimés dans le temps produits par chaque paire (32, 34; 34, 36; 36, 32) desdites mémoires, et pour appliquer à une borne de sortie, une ligne à la fois, les signaux vidéo comprimés dans le temps et dont la moyenne est faite qui alternent avec des signaux vidéo comprimés dans le temps et non interpolés qui sont dérivés des mémoires.

3. Processeur selon la revendication 1, où ledit moyen de sortie comprend au moins un circuit faisant la moyenne (60, 66) et au moins un commutateur (54) couplés auxdites mémoires pour former un signal vidéo traité de sortie où des lignes comprimées dans le temps et non interpolées dérivées desdites mémoires alternent avec des lignes qui sont comprimées dans le temps et formées en faisant la moyenne.

4. Processeur selon la revendication 2 ou 3, où ledit moyen de sortie comprend un circuit séparé formant la moyenne (60/66; 62/68; 64/70) pour chaque paire (32/34; 34/36; 36/32) desdites trois mémoires.

5. Processeur selon la revendication 3, où ledit moyen de sortie comprend trois circuits formant la moyenne (60/66; 62/68; 64/70) connectés entre les paires respectives (32/34; 34/36; 36/32) desdites mémoires et où ledit commutateur (54) a trois entrées qui sont couplées à des mémoires respectives (32, 34, 36), trois autres entrées couplées à des circuits respectifs de formation de la moyenne et une sortie où il produit le signal vidéo traité de sortie avec ses lignes alternées consistant en lignes comprimées dans le temps non interpolées dérivées desdites mémoires et avec des lignes intermédiaires consistant en lignes comprimées dans le temps et dont la moyenne est faite, qui sont obtenues desdits circuits formant la moyenne.

6. Processeur selon la revendication 1, où ledit moyen de sortie comprend uniquement un circuit de formation de la moyenne (82/84) ayant des première et seconde entrées et, couplés auxdites entrées, des commutateurs respectifs (54A, 54B) servant à coupler sélectivement lesdites entrées aux sorties desdites mémoires pour former ledit signal vidéo traité de sortie avec ses lignes alternées consistant en lignes comprimées dans le temps non interpolées et avec des lignes intermédiaires consistant en lignes comprimées dans le temps et dont la moyenne est faite qui sont obtenues dudit circuit formant la moyenne.

7. Processeur selon la revendication 6, comprenant un moyen de commande de commutateur pour commander les commutateurs pour sélectivement coupler les deux entrées dudit circuit formant la moyenne à l'une des deux mémoires qui sont lues pendant un premier intervalle de temps et pour coupler lesdites entrées dudit circuit formant la moyenne à certaines respectives des deux mémoires qui sont lues pendant un second intervalle de temps pour produire ledit signal vidéo de sortie du circuit formant la moyenne sous la forme d'une combinaison de lignes non interpolées comprimées dans le temps, chacune obtenue d'une mémoire et, entrelacées avec celles-ci, des lignes comprimées dans le temps dont la moyenne est faite, chacune étant obtenue des deux mémoires.

8. Processeur selon la revendication 7, où chacun desdits commutateurs (54A, 54B) a trois entrées, chaque entrée étant connectée à une mémoire respective (32, 34, 36) et une sortie connectée à l'entrée respective dudit circuit (82/84) formant la moyenne; et ledit moyen de commande de commutateur comprend un générateur de signaux de temporisation (figure 5) pour commander lesdits commutateurs pour coupler l'un desdits deux signaux vidéo comprimés dans le temps aux deux entrées dudit circuit de formation de la moyenne du signal pendant un premier intervalle de temps et pour coupler lesdits deux signaux vidéo comprimés dans le temps à des entrées respectives dudit circuit de formation de la moyenne pendant un second intervalle de temps.