METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a method of manufacturing a MOS integrated circuit (IC) device which is constructed of MOS (Metal Oxide Semiconductor) type transistors.

CMOS (Complementary MOS) ICs, which have MOS transistors of the two opposite channel conductivity types of P- and N-channels, have such merits as very low power dissipation and high operating speed and are used for various circuits.

The following method of manufacturing CMOS ICs has been generally used. First, a polycrystalline silicon film which will become gate electrodes is formed on an N-type silicon semiconductor substrate and a P-type well region formed therein. The P-type well region is selectively covered with a silicon dioxide film (SiO_2 film) formed by chemical vapor deposition (CVD). Using the SiO_2 film as a mask, boron is diffused into the N-type silicon substrate not covered with the SiO_2 film, to form source and drain regions of the P^+-type. Thereafter, the SiC_2 film is removed, that part of the surface of the N-type silicon semiconductor substrate

in which the P-type well region is not formed is selectively covered with another SiO_2 film formed by CVD, and using this SiO_2 film as a mask, phosphorus is diffused into the surface of the P-type well region so as to form source and drain regions of the N-type. The SiO_2 film formed by the CVD and used as the mask at the phosphorus diffusion stage is removed. A new SiO_2 passivation film is formed on the whole surface of the substrate by CVD. Contact holes are formed in the new SiO_2 film, and an Al film is evaporated on the whole surface and subsequently formed into Al electrodes by photolithography.

This method, however, has been found by the inventors to have the following problem. When the SiO_2 film formed by the CVD is removed by etching, the underlying field SiO_2 film is also etched partly. Consequently, a step arises in the surface of the field SiO_2 film. If Al wiring or the like is then formed over the field SiO_2 film, there is posed the problem that the Al wiring is liable to breakage at the step. The breakage of the Al wiring occurs noticeably particularly when wiring made of a polycrystalline silicon film is formed on the field SiO_2 film. The reason is that, when the SiO_2 film formed by the CVD is etched, the field SiO_2 film under the wiring of the polycrystalline silicon film is side-etched (under-etched), so that the step of the

field SiO_2 film surface in this part (the distance from the surface of the wiring of the polycrystalline silicon film to the side-etched surface of the field SiO_2 film) becomes more abrupt (longer). Therefore breakage of the wiring due to the step is more liable to take place.

On the other hand, in recent years, researches have been made on the application of a double layer structure of polycrystalline silicon films to a CMOS IC. The inventors studied and produced a CMOS IC of the double layer structure by the use of the conventional manufacturing method described above. As a result, they encountered the following problems. The second layer of polycrystalline silicon film deposited over the step part of the surface of the field SiO_2 film as described above is not sufficiently removed when etched in order to photolithographically work it into a predetermined pattern. Due to the deposited polycrystalline silicon film, a leakage current flows between the wiring leads of the second layer (level) of polycrystalline silicon film. One possible measure considered for solving the problem was to render the wiring pitches of the polycrystalline silicon film large. This measure, however, requires a large wiring area and results in hampering enhancement in the density of integration.

Further, if one intends to manufacture a CMOS IC which has a double-layer structure of polycrystalline silicon films, there is the problem that the conventional method of manufacturing the CMOS IC as described above is a complicated process. The reason is that, as explained before, the SiO_2 films formed by the CVD are respectively used as the masks in the step of forming the N^+-type source and drain regions and the step of forming the P^+-type source and drain regions, and besides these SiO_2 films which serve as the masks, a further SiO_2 film formed by CVD is used as the inter-layer insulator film between the first layer of polycrystalline silicon film and the second layer of polycrystalline silicon film.

Therefore, according to the present invention there is provided a method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor body having a first semiconductor region of a first conductivity type and a second semiconductor region of a second conductivity type;

(b) covering the first semiconductor region with a first mask;

(c) introducing impurity of the first conductivity type selectively into the second semiconductor region using the first mask;

(d) covering the second semiconductor region with a second mask which has different etching characteristics from the first mask, the second mask being formed at least in part by deposition;

(e) removing the first mask, other than any parts covered by the second mask, by etching; and

(f) introducing an impurity of the second conductivity type into the first semiconductor region using the second mask.

(g) using at least part of the second mask as an insulating layer between a conductive layer and the semiconductor body.

An embodiment of the invention will now be described in detail, by way of example, with reference to the accompanying drawings in which:

Figures 1A to 1N show the sectional structures of a CMOS IC at various steps in order to elucidate a method of manufacturing a semiconductor device according to an embodiment of the present invention.

First, as shown in Figure 1A, one major surface of a silicon semiconductor substrate 1 of a first conductivity type, e. g., the N^- type (resistivity: 8 - 12 Ω-cm) is thermally oxidized to grow a silicon dioxide film (SiO_2 film) 2 having a thickness of 430 Å. A silicon nitride film (Si_3N_4 film) is formed on the SiO_2 film 2 by CVD and patterned by photolithography, to form an oxidation impermeable mask made of the Si_3N_4 film 3.

Subsequently, using the mask of the Si_3N_4 film 3, ions of an impurity of the first conductivity type or N type, e. g., ions of phosphorus are implanted into the surface of the substrate 1 under conditions of 125 keV and 2 x $10^{12}/cm^2$. As a result, an ion-implanted layer 4 is formed. Further, using the Si_3N_4 film 3 as a mask, that region of the major surface of the substrate in which the ion-implanted layer 4 is formed is locally oxidized thermally. Thus, the part of the major surface of the substrate is covered with an SiO_2 film 5 which is 1200 Å thick, as shown in Figure 1B.

Subsequently, the Si_3N_4 film 3 is removed by etching. Further, ions of an impurity of a second conductivity type or the P type, e. g., ions of boron fluoride BF_2 indicated at numeral 6 are implanted under conditions of 60 keV and $3 \times 10^{12}/cm^2$. Here, the difference between the thicknesses of the SiO_2 film 2 and the SiO_2 film 5 is utilized, and a boron-implanted layer 7 is formed only under the thin SiO_2 film 2 as shown in Figure 1C.

At the next step, the impurities of the ion-implanted layers 4 and 7 are diffused deep by a heat treatment at 1200 °C for 6 hours in a non-oxidizing atmosphere, e. g., nitrogen (N_2) gas. As a result, a first semiconductor region comprising an N-type well region 8 and a second semiconductor region comprising a P^--type well region 9 are respectively formed as shown in Figure 1D. The first well region 8 serves to form a MOSFET of a second channel conductivity type or the P channel conductivity type, while the second well region 9 serves to form a MOSFET of a first channel conductivity type or the N channel conductivity type. Thereafter, an oxidation impermeable Si_3N_4 film 10 is deposited on the whole surface by CVD.

Subsequently, as shown in Figure 1E, the Si_3N_4 film 10 is worked by photolithography into a pattern which determines regions for forming the elements. Further, ions of a P-type impurity, e. g., boron fluoride BF_2

indicated at numeral 11 are implanted into the silicon substrate 1 through only the thin SiO_2 film 2 under conditions of 60 keV and $3 \times 10^{13}/cm^2$. At this time, the Si_3N_4 film 10 and the SiO_2 film 5 serve as a mask. Thus, an ion-implanted layer 12 for a channel stopper is formed.

At the next step, using the Si_3N_4 film 10 as a mask, the silicon substrate is locally oxidized thermally, to grow a field SiO_2 film 14 being about 9500 Å thick on selected areas. Simultaneously therewith, the impurity of the ion-implanted layer 12 is diffused to form a P-type channel stopper region 13. Thereafter, the Si_3N_4 film 10 is removed by etching, and also the SiO_2 films 2 and 5 underlying the Si_3N_4 film 10 are removed by etching. As a result, those parts of the surface of the N-type silicon semiconductor substrate which correspond to the element forming regions are exposed. By thermally oxidizing the exposed surface parts, gate oxide films 15 which are about 350 Å thick are formed on the areas from which the Si_3N_4 film 10 and the SiO_2 films 2, 5 have been removed. This state is shown in Figure 1F. The portions of the P^--type well region 9 and N-type well region 8 underlying the gate oxide films 15 shall be called the element forming regions.

Next, a first-level polycrystalline silicon film

4000 Å thick is deposited on the whole surfaces of the element forming regions and the field SiO_2 film 14 by CVD. Phosphorus is introduced into this polycrystalline silicon film as an impurity, to render it low in resistivity. Thereafter, the polycrystalline silicon film is patterned by photolithography into polycrystalline silicon layers to become the gate electrodes 16, 17 of the respective MISFETs and a first-level polycrystalline silicon wiring lead 18 as shown in Figure 1G. Boron ions for controlling the threshold voltages V_{th} of the MISFETs may well be implanted into the surfaces of the element forming regions before forming the polycrystalline silicon layers.

Subsequently, steam oxidation is conducted at 875 °C for 10 minutes, to form silicon dioxide films 23 which are about 400 Å thick on the surfaces of the polycrystalline silicon layers 16, 17 and 18.

Next, an Si_3N_4 film 19 is formed on the P^--type well region 9 and N-type well region 8 (on the whole surface of the substrate) by CVD. This film may be a film which differs in property from the underlying insulator film, i. e., field SiO_2 film. In other words, it may have an etching rate unequal to that of the field SiO_2 film. Using photoresist layers as a mask, the Si_3N_4 film 19 is selectively removed by a plasma etching process employing $CF_4 + O_2$ gas, so as to be patterned into a

predetermined shape. At this time, owing to the unequal etching rates, the underlying films of the field SiO_2 film 14 etc. are not etched. Thus, a first mask which covers the N-type well region 9 is formed from the Si_3N_4 film 19, for use when introducing an N-type impurity into the substrate. Using this first mask formed from the Si_3N_4 film 19, an ion beam 20 of an N-type impurity, preferably arsenic, is projected into the P^--type well region 9 under conditions of 80 keV and $10^{16}/cm^2$. Then, arsenic-implanted layers 21 and 22 which will become source and drain regions are formed in the surface parts of the P^--type well region 9 located on both the sides of the gate electrode 17. This state is shown in Figure 1H. As a process for introducing this impurity, ion implantation is favorable, but diffusion may well be resorted to. In this case, the SiO_2 film 15 on the surface parts of the P^--type well region 9 to become the source and drain regions needs to be selectively removed at or before the diffusion.

Subsequently, as shown in Figure 1I, an SiO_2 film 24 is formed on the whole surfaces of the N-type well region 8 and P^--type well region 9 (on the whole surface of the substrate) by CVD. This film is used as an inter-layer insulator film between first-level and second-level polycrystalline silicon layers. It may well be replaced with a phosphosilicate glass (PSG) film. Essentially, the film 24 may differ

in the etching rate from the underlying Si_3N_4 film 19. Thus, when the Si_3N_4 film 19 is removed, the film to be used as the inter-layer insulator film is prevented from damaging, likewise to the field SiO_2 film 14.

As shown in Figure 1J, only that part of the SiO_2 film 24 which overlies the N-type well region 8 is removed by etching by the use of an etchant containing HF and NH_4F at a mixing ratio of 1 : 6. Next, the Si_3N_4 film 19 underlying the part is removed by a plasma etching process employing $CF_4 + O_2$ gas. Herein, the end part of the SiO_2 film 24 remaining unetched should desirably lie on the remaining part of the Si_3N_4 film 19 as shown in Figure 1J. In this way, a step is reliably prevented from appearing in the field SiO_2 film 14 on account of the etching of the SiO_2 film 24. By annealing the resultant structure in a non-oxidizing atmosphere, e. g., nitrogen atmosphere, the impurity of the arsenic-implanted layers 21, 22 is subjected to drive-in diffusion, to form the source region 25 and drain region 26 of the N type. Thus, the N channel type MOSFET which is the first channel conductivity type MOSFET is completed. Further, using as a second mask the SiO_2 film 24 which is left on the P^--type well region 9, the surface of the N-type well region 8 is irradiated with boron ions 27 under conditions of 30 keV and $1.5 \times 10^{15}/cm^2$. Using the

gate electrode 16 and the SiO_2 film 23 on the side surface thereof as a mask, boron-implanted layers 28 and 29 which will become source and drain regions are respectively formed on both the sides of the gate electrode 16.

After the SiO_2 films 24, 23 and 15 overlying the source region 25 and drain region 26 and the polycrystalline silicon wiring lead 18 have been selectively removed by photolithography, a second-level polycrystalline silicon film 30 is deposited on the whole surface to a thickness of 2000 Å by CVD as shown in Figure 1K.

Subsequently, the polycrystalline silicon film 30 is worked by photolithography to form the second-level polycrystalline silicon layers 31, 32, 33 and 34 as shown in Figure 1L. The polycrystalline silicon layers 31 and 34 are rendered low in resistivity by introducing an impurity, e. g., phosphorus and are used as wiring leads. The wiring leads of the second-level polycrystalline silicon film such as the polycrystalline silicon layers 31 and 34 are disposed on only the P-type well. Parts of the polycrystalline silicon layers 31 and 34 can be used as high resistance elements without introducing the impurity. No impurity is introduced into the polycrystalline silicon layers 32 and 33. These layers are rendered low in resistivity by the diffusion of Al atoms from Al wiring which is connected by a later

step. The formation of contact holes is facilitated owing to the provision of the polycrystalline silicon layers 32 and 33.

Subsequently, as shown in Figure 1M, an SiO_2 film 35 and a phosphosilicate glass film 36 are deposited by CVD, whereupon they are worked by photolithography to form contact holes 40, 41, 42, 43 and 44. Thereafter, annealing at 950 ^{o}C for 20 minutes is performed in a nitrogen atmosphere.

By this annealing, the boron-implanted layers 28 and 29 undergo drive-in diffusion, and the source region 37 and drain region 38 of the P type are formed. Thus, the P-channel type MOSFET which is the second channel conductivity type MOSFET is completed.

Subsequently, as shown in Figure 1N, aluminum is deposited by vacuum evaporation and is worked by photolithography to form aluminum wiring leads 50, 51, 52, 53 and 54. Further, after annealing the resultant structure at 450 ^{o}C in hydrogen gas H_2 for 60 minutes, the whole surface is covered with a final passivation film, e. g., a silicon nitride film formed by plasma CVD. The manufacturing process is thus completed.

The Si_3N_4 film 19 which differs in etching rate from the field SiO_2 film 14 is used as the first mask at the time at which

the N-type impurity is ion-implanted into the second well region 9 of the P^- type as in the step illustrated in Figure 1H. Therefore, when the Si_3N_4 film 19 is removed, the underlying field SiO_2 film 14 is not etched. Moreover, the CVD SiO_2 film 24 which serves as the second mask for the ion implantation of the P-type impurity into the first well region 8 of the N type is left as the inter-layer insulator film even after the ion implantation of the P-type impurity. Therefore, the underlying field SiO_2 film 14 is not etched. Accordingly, no step develops in the surface of the field SiO_2 film 14, so that breakage of the Al wiring lead formed over the SiO_2 film, attributable to the step, can be prevented, and no leakage current occurs between the polycrystalline silicon wiring leads. Further, the process does not involve the complication of forming a new inter-layer insulator film after removing the second mask used for the introduction of the P-type impurity as in the prior art. Especially in forming a CMOS IC having a double-layer structure of polycrystalline silicon, the method described is effective because it can be formed without complicating the process.

The present invention is not restricted to the foregoing embodiment, but can be variously modified. By way of example, while the embodiment has been explained

with reference to a double-layer structure employing polycrystalline silicon films, the present invention is also applicable to the case of forming a multilayer structure having films of a material other than polycrystalline silicon, for example, a multilayer structure including layers of refractory metals such as molybdenum and tantalum or a multilayer structure including a refractory metal layer and a polycrystalline silicon film. In addition, the embodiment has been explained as to the case of first performing the ion implantation of the N^+-type impurity to form the N-channel type MOSFET being the first channel conductivity type MOSFET and thereafter performing the ion implantation of the P^+-type impurity to form the P-channel type MOSFET being the second channel conductivity type MOSFET. However, the reverse case is also possible where, after forming the source and drain regions of a P-channel type MOSFET as the first channel conductivity type MOSFET, the source and drain regions of an N-channel type MOSFET as the second channel conductivity type MOSFET are formed. In this case, an insulator film formed on the P-channel type MOSFET is used as a mask for forming the source and drain regions of the N-channel type MOSFET, and it is left intact and is used as an inter-layer insulator film.

The Si_3N_4 film 19 shown in Figure 1H may well be

replaced with a polycrystalline silicon film. Essentially, the film 19 may differ in the etching rate from the underlying field SiO_2 film.

In the step illustrated in Figure 1H, the oxide film which is formed on the surfaces of the polycrystalline silicon films 16, 17 and 18 may be an SiO_2 film formed by CVD, instead of the thermal oxidation film formed by the steam oxidation described before. Since, however, this SiO_2 film formed by the CVD is liable to overetching, the thermal oxidation film is more favorable.

As the material 24 of the second mask shown in Figure 1I, it is necessary to select a film which can be used as the inter-layer insulator film and which is good in coverage and in quality. While the SiO_2 film formed by the CVD as mentioned in the foregoing embodiment is a favorable material, a PSG film is also exemplified as being favorable. Since Si_3N_4 film traps charges at an interface, it is not favorable as the inter-layer insulator film. In addition, the steps illustrated in Figures 1I and 1J may well be carried out by an expedient as stated below. After the N-type impurity ions 20 have been implanted into the surface of the P^--type well region 9 by employing the Si_3N_4 film 19 as the first mask as illustrated in Figure 1H, the Si_3N_4 film 19 is removed with hot phosphoric acid,

whereupon the SiO_2 film 24 for forming the second mask is formed by CVD on the whole surfaces of the N-type well region 8 and P^--type well region 9. Thereafter, the SiO_2 film 24 on the N-type well region 8 is selectively removed to obtain substantially the same structure as shown in Figure 1J.

The present invention described above is effective particularly when applied to a static RAM in which a memory cell is constructed of N-channel type MOSFETs within a P-type well region and load resistors made of a polycrystalline silicon film, and a CMOS circuit is used for a peripheral circuit, to render the power dissipation low, as shown in Japanese Patent Application No. 56-15733. In this case, the load resistors of the memory cell and wiring therefor are formed of the second-level polycrystalline silicon layer. Herein, a polycrystalline silicon layer to form the gate electrode of a MOSFET which constitutes the CMOS circuit of the peripheral circuit is formed simultaneously with the first-level polycrystalline silicon layer which forms the MOSFETs for the memory cells. The second-level polycrystalline silicon layer is unnecessary in the peripheral circuit. As the insulator film between the second-level polycrystalline silicon layer and the first-level polycrystalline silicon layer which is the gate electrode of the N-channel type MOSFET of the memory

cell, a layer which forms a mask for the diffusion of a P-type impurity is used. Thus, a static RAM of low power dissipation can be formed without resorting to a complicated process. The invention is applicable, not only to the above static RAM, but also to a semiconductor integrated circuit device in which a CMOS circuit and bipolar transistors are formed on an identical substrate. Besides, the present invention is applicable to any semiconductor device formed of a CMOS circuit.

CLAIMS:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor body having a first semiconductor region of a first conductivity type and a second semiconductor region of a second conductivity type;

(b) covering the first semiconductor region with a first mask;

(c) introducing impurity of the first conductivity type selectively into the second semiconductor region using the first mask;

(d) covering the second semiconductor region with a second mask which has different etching characteristics from the first mask, the second mask being formed at least in part by deposition;

(e) removing the first mask, other than any parts covered by the second mask, by etching; and

(f) introducing an impurity of the second conductivity type into the first semiconductor region using the second mask.

(g) using at least part of the second mask as an insulating layer between a conductive layer and the semiconductor body.

2. A method according to claim 1, wherein the first and second semiconductor regions are isolated from each other by a thick oxide film formed by thermal oxidation of the body.

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3. A method according to claim 1 or claim 2, wherein the conductive layer is a first conductive layer, and the method further comprises the steps of:

(h) forming a gate oxide film after performing the step (a); and

(i) forming a second conductive layer selectively on the thin oxide film after performing said step (h), said first conductive layer serving as a mask when introducing the impurities at said steps (c) and (f) and also as gate electrodes; and wherein

(j) said step (c) includes impurity introduction for forming a source or drain region of a first channel conductivity type MOSFET;

(k) said step (f) includes impurity introduction for forming a source or drain region of a second channel conductivity type MOSFET.

4. A method according to claim 3, wherein the gate oxide film is formed by thermal oxidation of the body.

5. A method according to claim 3 or claim 4, wherein the first and/or second conductive layer is a polycrystalline silicon layer.

6. A method of manufacturing a semiconductor device according to any one of claims 3 to 5, wherein the first conductivity type is N type, the second conductivity type

MOSFET is an N-channel type MOSFET, and the second channel conductivity type MOSFET is a P-channel type MOSFET.

7. A method according to claim 6, wherein parts of the conductor layer have a low resistivity, and other parts thereof have a high resistivity.

8. A method according to claim 7, wherein the semiconductor device is used as a semiconductor memory which includes memory cells that are made of the N-channel type MOSFETs and the high resistivity parts of the conductor layer.

9. A method according to any one of claims 1 to 8, wherein the first mask is a silicon nitride film.

10. A method of manufacturing a semiconductor device according to any one of claims 1 to 9, wherein the second mask at least in part comprises an inorganic material.

11. A method according to any one of claims 1 to 10, wherein the second mask is a silicon dioxide film.

12. A method according to any one of claims 1 to 10, wherein the second mask is made of a phosphosilicate glass film.

13. A method according to any one of the preceding claims,

wherein the material for forming the second mask is deposited by chemical deposition.

14. A method according to claim 13, wherein the chemical deposition is chemical vapour deposition.

15. A method according to any one of claims 1 to 14, wherein the etching in step e) is performed by a plasma etching process.

16. A method according to claim 15, wherein the plasma etching process employs $CF_4 + O_2$ gas.

17. A method according to any one of the preceding claims, wherein part of the first mask is overlapped by part of the second mask.

18. A method according to claim 17, wherein the part of the first mask overlapped by the second mask remains after step e) and forms an inter-layer insulating film.

19. A method according to any one of the preceding claims, wherein some of the second mask is removed after step f), the remaining part of the second mask forming a passivation film.

20. A method of manufacturing a semiconductor device,

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substantially as described herein with reference to the accompanying drawings.