

CIRCUIT FOR GENERATING INTERNAL SUPPLY VOLTAGE

The present invention relates to circuits for generating internal supply voltages, particularly although not exclusively for use in high density
5 semiconductor memory devices.

At the present time, in a semiconductor memory device with high memory capacity, it is often required to supply a MOS transistor below a micron unit level with a low supply voltage lower than an external supply
10 voltage of 5V which is generally supplied in computer systems. To this end, an internal supply voltage generator must be prepared in semiconductor chips, in addition to a memory circuit, so as to supply the low internal supply voltage. For instance, a semiconductor DRAM device over 16Mbit level necessarily includes such an internal supply voltage generator in order to
15 obtain high reliability of the memory device.

A prior art internal supply voltage generator and the characteristics thereof are disclosed with reference to Figures 1 to 3 of the accompanying
20 drawings.

Referring to Figure 1, a conventional internal supply voltage generator 100 is comprised of a reference voltage generator 50, a comparator 60 and an output circuit 70. Shown in Figure 2 are the characteristics of the internal supply voltage generator of Figure 1, in comparison with the external supply
25 voltage. An alternative embodiment of the reference voltage generator 50 of Figure 1 is shown in Figure 3.

Referring again to Figure 1, the internal supply voltage generator 100 has the reference voltage generator 50 and the output circuit 70 which is comprised of a PMOS transistor 10 serving as a variable resistor. The voltage outputs from the reference voltage generator 50 and the output circuit 70 are compared at the comparator 60, which is a differential amplifier for controlling the voltage applied to the gate of the PMOS transistor 10. The reference voltage generator 50 has first and second resistors R_1 , R_2 connected in series between the external supply voltage $V_{cc_{ext}}$ and the ground level, to generate reference voltage V_{ref} through a connection node 3. The comparator 60 has first and second NMOS transistors 6, 7 forming a differential amplifier, a third NMOS transistor 8 serving as a constant current source, and first and second PMOS transistors 4, 5 forming a current mirror load stage. Moreover, the PMOS transistor 10 has its source connected to the external supply voltage $V_{cc_{ext}}$, and the drain connected to the internal supply voltage $V_{cc_{int}}$ of an output node 11. In the drawing, the reference voltage V_{ref} is applied to the gate of the first NMOS transistor 6 of the comparator 60. In the event that a load current flows from the output node 11 to a memory circuit (not shown), a voltage drop occurs at the PMOS transistor 10 of the output circuit 70. As a result, the internal supply voltage is set to a voltage level lower than the external supply voltage. At the same moment, the comparator 60 controls the gate voltage of the PMOS transistor 10 so as to keep the internal supply voltage level identical to the reference voltage V_{ref} level.

The internal supply voltage generator 100 should keep a constant internal supply voltage regardless of the change of the external supply voltage in order to obtain high reliability of the semiconductor memory device. Undesirably, however, the conventional internal supply voltage generator 100

of Figure 1 typically has a voltage difference ΔV as shown in Figure 2, in response to the increase of the external supply voltage. The foregoing problem is caused by the fact that the reference voltage V_{ref} from the reference voltage

generator 50 is $V_{ref} = \frac{R_2}{(R_1 + R_2)} V_{CC_{ext}}$. Therefore, the reference voltage V_{ref}

5 increases as the external supply voltage increases, thereby increasing the internal supply voltage. Accordingly, the reliability of the semiconductor memory device may be reduced.

Referring to Figure 3, an alternative reference voltage generator 50 is
10 comprised of first to third PMOS transistors 12, 13, 14 connected in series, and fourth and fifth PMOS transistors 15, 16 connected in series, the first to third PMOS transistors being connected in parallel to the fourth and fifth PMOS transistors. The gates and drains of the first to fifth PMOS transistors 12 - 16 are each diode-connected and, further, the gate of the fourth PMOS
15 transistor 15 is connected to the source of the third PMOS transistor 14. The source of the third PMOS transistor 14 is so coupled as to set the gate voltage level of the fourth PMOS transistor 15 to $\frac{V_{CC_{ext}}}{3}$, the source of the fourth

PMOS transistor 15 becoming an output node 17, by which the reference voltage generator 50 generates the reference voltage V_{ref} through the output
20 node 17. As the temperature increases, however, the threshold voltage V_{th} of the respective PMOS transistors in the reference voltage generator 50 shown in Figure 3 is reduced. Therefore, the reference voltage V_{ref} will also be reduced. If the reference voltage is reduced, the internal supply voltage will

also be reduced, causing the semiconductor memory device to operate at a low speed.

Preferred embodiments of the present invention aim to provide a circuit
5 for generating an internal supply voltage which allows a semiconductor memory device to operate at a stable, constant speed regardless of changes of temperature, wherein the output voltage thereof has a tendency to increase as the temperature increases.

10 According to the present invention, there is provided a circuit for receiving an external supply voltage and for generating an internal supply voltage lower than said external supply voltage, for use in a semiconductor memory device, the circuit comprising:

15 a reference voltage generating means connected to receive said external voltage, for generating a reference voltage;

a comparator means connected to receive the output of said reference
voltage generating means, for comparing a signal applied from a first input
20 line with a signal from a second input line, the first input line being coupled to the output of said reference voltage generating means;

an output means receiving the output of said comparator means, for
generating at an output node thereof said internal supply voltage; and

25 a voltage sharing means for receiving the output of said output means, and supplying an output to the second input line of said comparator means:

wherein the output of said output means has a tendency to increase in response to increase of the temperature, thus compensating for a decrease in the reference voltage caused by the increase in temperature, to provide an output which is substantially independent of temperature.

Preferably, said reference voltage generating means comprises:

a first resistor one end thereof being connected to an output node of said reference voltage generator;

a first bipolar transistor of which a collector and base are commonly coupled to the other end of the said first resistor and of which an emitter is coupled to a ground level;

a second resistor one end thereof being connected to the output node of said reference voltage generator;

a second bipolar transistor of which a collector is coupled to the other end of said second resistor and of which a base is coupled to the collector of said first bipolar transistor;

a third resistor, one end thereof being coupled to an emitter of said second bipolar transistor, the other end thereof being coupled to said ground level; and

a third bipolar transistor of which a collector is coupled to the output node of said reference voltage generator, and of which a base is coupled to the collector of said second bipolar transistor, of which the emitter is coupled to said ground level.

Preferably, said comparator means comprises:

a first PMOS transistor of which a source is coupled to said external supply voltage;

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a second PMOS transistor of which a source is coupled to said external supply voltage and of which a gate and drain are commonly coupled to a gate of said first PMOS transistor;

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a first NMOS transistor of which a gate is coupled to the first input line and of which a drain is coupled to a drain of said first PMOS transistor;

a second NMOS transistor of which a gate is coupled to the second input line, and of which a drain is coupled to the drain of said second PMOS transistor;

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a third NMOS transistor of which a gate is coupled to the first input line, a source is coupled to said ground level, and of which a drain is coupled to sources of the first and second NMOS transistors; and

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an output node formed at a connection of the drains of the first PMOS transistor and the first NMOS transistor.

Preferably, said output means comprises:

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a PMOS transistor of which a source is coupled to the external supply voltage, and of which a gate is coupled to the output node of said comparator means; and

5 an output node coupled to a drain of said PMOS transistor.

Preferably, said voltage sharing means tends to increase said internal supply voltage in response to increase of temperature, said voltage sharing means comprising:

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first and second variable resistor means coupled in series between said output means and a ground level, and having

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an output node formed at a connection of said first and second variable resistor means.

Preferably, a resistance increase ratio in response to increase of the temperature, of said first variable resistor means, is higher than that of said second variable resistor means.

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Preferably, said first and second variable resistor means comprises:

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a first MOS transistor having an end of a channel thereof coupled to said output means, and another end of the channel and a gate thereof being diode-connected; and

a second MOS transistor having an end of a channel thereof coupled to said output node, and another end of the channel and a gate thereof being diode-connected to said ground level:

- 5 said first MOS transistor having a channel longer in length than that of said second MOS transistor.

Preferably, said voltage sharing means comprises:

- 10 a first PMOS transistor of which a source is coupled to the output node of said output means, and of which a gate and drain are diode-connected;

- a second PMOS transistor of which a source is coupled to the drain of said first PMOS transistor, and of which a gate and drain are diode-connected
15 to said ground level; and

an output node formed at a common connection of the first and second PMOS transistors.

- 20 The invention also extends to a semiconductor memory device provided with a circuit according to any of the preceding aspects of the invention.

- For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example,
25 to Figures 4 to 7 of the accompanying diagrammatic drawings, in which:

Figure 4 shows one example of an internal supply voltage generator embodying the present invention;

5 Figure 5 shows output characteristics of the internal supply voltage generator of Figure 4;

Figure 6 shows one example of an embodiment of the internal supply voltage generator of Figure 4, in more detail; and

10 Figure 7 is a table illustrating decrease ratio of the current driving power of MOS transistors in response to change of temperature.

In Figures 4 and 6, like reference numerals denote parts corresponding to those shown in Figures 1 and 3.

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Referring to Figure 4, there is shown a voltage sharing circuit 80 connected to a comparator 60 and an output circuit 70. A reference voltage generator 50, to which an external supply voltage is applied, generates a reference voltage V_{ref} . The comparator 60, connected to the output of the reference voltage generator 50, compares a first input voltage coupled to the reference voltage V_{ref} with a second input voltage. The output of the comparator 60 is coupled to an input terminal of the output circuit 70 for generating internal supply voltage $V_{cc_{int}}$. The voltage sharing circuit 80, connected to the output circuit 70, generates the second input voltage at an output node thereof, to thereby allow the output voltage level of the output circuit 70 to increase in response to increase of temperature. It should be further noted that the voltage sharing circuit 80 has first and second variable

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load resistors R_1' , R_2' of which resistances increase in response to increase of temperature, wherein resistance of the first variable load resistor R_1' is higher than that of the second variable load resistor R_2' . Furthermore, the resistance increase ratio, according to increase of temperature, of the first variable load resistor R_1' is higher than that of the second variable load resistor R_2' .

The output voltage $V_{CC_{int}}$ of the internal supply voltage generator 100 of Figure 4, can be written as $V_{CC_{int}} = \frac{1 + R_1'}{R_2'} \cdot V_{ref}$, where the ratio of resistance variation to temperature change is $R_1' > R_2'$. It is therefore apparent from the foregoing that as the temperature increases, the resistance increase ratio of the first variable load resistor R_1' becomes higher than that of the second variable load resistor R_2' , thereby increasing the internal supply voltage $V_{CC_{int}}$.

As is illustrated with reference to Figure 5, it is to be understood that the internal supply voltage $V_{CC_{int}}$ increases stably to keep it constant as the temperature increases. Accordingly, the problem found in conventional circuits, that as the temperature increases, the reference voltage V_{ref} of the reference voltage generator is reduced, resulting in the undesirably low internal supply voltage, as well as the problem that as the external supply voltage increases, the reference voltage also increases, resulting in an unstable internal supply voltage, are both solved.

An example of an embodiment of the internal supply voltage generator 100 of Figure 4 will now be described in more detail hereinbelow, with reference to Figure 6.

5 The reference voltage generator 50 has a constant current source 31, an input thereof being coupled to the external supply voltage $V_{cc_{ext}}$, an output node 38 being coupled to the output of the constant current source 31, and a circuit connected between the output node and the ground level, for dropping the voltage level of the output node 38 to a predetermined level.

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 The voltage dropping circuit has a first resistor 35 connected to the output node 38, another end of the first resistor 35 being commonly coupled to the collector and base of a first bipolar transistor 32 of which the emitter is coupled to ground level. A second resistor 36, an end thereof being coupled to the output node 38, is coupled to the collector of a second bipolar transistor 33 having its base coupled to the collector of the first bipolar transistor 32 and its emitter connected to ground level via a third resistor 37. Moreover, the output node 38 is connected to the collector of a third bipolar transistor 34 of which the base is connected to the collector of the second bipolar transistor 33 and the emitter is coupled to the ground level.

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 The comparator 60 has a first PMOS transistor 39 of which the source is connected to the external supply voltage $V_{cc_{ext}}$, and a second PMOS transistor 40 of which the source is connected to the external supply voltage.

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 The gate of the first PMOS transistor 39 is commonly connected to the gate and drain of the second PMOS transistor 40. The gate of a first NMOS transistor 41 is coupled to a first input voltage, i.e. the reference voltage V_{ref} .

Furthermore, the first NMOS transistor 41 has a drain connected to the drain of the first PMOS transistor 39 and a source connected to the source of a second NMOS transistor 43 of which the drain is connected to the drain of the second PMOS transistor 40 and the gate is coupled to a second input voltage.

- 5 The sources of the first and second NMOS transistors 41, 43 are connected to the drain of a third NMOS transistor 42 of which the source is connected to ground level and the gate is coupled to the first input voltage. The connection node 44 of the drains of the first PMOS transistor 39 and the first NMOS transistor 41 serves as an output node of the comparator 60.

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The output circuit 70 is comprised of a PMOS transistor with the source being connected to the external supply voltage $V_{cc_{ext}}$ and the gate being connected to the output node 44 of the comparator 60. The drain of the PMOS transistor 45 is connected to an output node 49 through which the internal supply voltage $V_{cc_{int}}$ is generated.

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The voltage sharing circuit 80 is comprised of a first PMOS transistor 46 with its source being connected to the output node 49 of the output circuit 70, and the gate and drain being diode-connected. A second PMOS transistor 47 has its source connected to the drain of the first PMOS transistor 46, and the gate and drain diode-connected to the ground level. Moreover, an output node 48 to which the drain and source of the first and second PMOS transistors are respectively connected, is coupled to the second input voltage.

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- 25 In order to generate a constant reference voltage V_{ref} regardless of change of temperature, the reference voltage generator 50 is comprised of bipolar transistors. For reference, the output voltage of the reference voltage

generator 50 is $V_{ref} = V_{BE} + \frac{R_b}{R_c} \cdot V_t \cdot \ln\left(\frac{I_1}{I_2} \cdot \frac{I_{s2}}{I_{s1}}\right)$, where V_{BE} is the base-

emitter voltage of the third bipolar transistor 34; V_t the thermoelectric voltage; R_b and R_c the resistances of the second and third resistors 36, 37 respectively; and I_{s1} and I_{s2} the collector saturation currents of the first and second bipolar transistors 32, 33 respectively. The reference voltage generator 50 is made such that the base-emitter voltage V_{BE} with a negative temperature coefficient of $-2.2\text{mV}/^\circ\text{C}$ and the thermoelectric voltage V_t with a positive temperature coefficient of $0.085\text{mV}/^\circ\text{C}$ are combined with each other so as to obtain a zero temperature coefficient. Therefore, unlike a conventional reference voltage generator using PMOS transistors having a negative temperature coefficient of $-3\text{mV}/^\circ\text{C}$, the reference voltage generator 50 of Figure 6 can generate a stable, constant reference voltage V_{ref} regardless of change of the temperature.

Further, the voltage sharing circuit 80 is so connected as to increase the reference voltage V_{ref} to thereby increase the internal supply voltage $V_{cc_{int}}$ according to increase of temperature. To this end, the channel conductance

$g_1 \left(= \frac{\partial I_{DS}}{\partial V_{DS}} \right)$ of the first PMOS transistor 46 is made lower than the channel

conductance g_2 of the second PMOS transistor 47. Therefore, the channel resistance of the first PMOS transistor 46 is higher than that of the second PMOS transistor 47, since conductance is of course a reciprocal of the resistance. From the foregoing, it can be understood that the current driving power is reduced for a MOS transistor with a high channel resistance. In general, a MOS transistor with a long channel length is under greater influence

of temperature than a MOS transistor with a short channel length; therefore, variation of the channel resistance according to the temperature, of the MOS transistor with a long channel length is comparatively considerable.

- 5 The internal supply voltage generator 100 of Figure 6 operating at a normal temperature of 25°C will now be considered hereinbelow.

10 The reference voltage V_{ref} from the reference voltage generator 50 is applied to the gates of the first and third NMOS transistors 41, 42. At this moment, if this voltage is higher than the voltage applied to the gate of the second NMOS transistor 43 of the comparator 60, a given voltage will be charged at the output node 49 of the output circuit 70. In the meantime, in the case where the reference voltage V_{ref} is at the same level as the output voltage of the voltage sharing circuit 80, the internal supply voltage $V_{cc_{int}}$ is
15 maintained constant by the voltage sharing circuit 80. In a little while, if the temperature is increased to over 83°C, the current flow in the first PMOS transistor 46 of the voltage sharing circuit 80 will be reduced. Therefore, a voltage lower than that at the normal temperature is applied to the gate of the second NMOS transistor 43 of the comparator 60. Thus, a voltage at the
20 output node 44 of the comparator 60 is charged to be lower than that during normal temperature and, thereby, a voltage at the output node 49, i.e. the internal supply voltage $V_{cc_{int}}$, of the output circuit 70 will be increased. Furthermore, as the temperature increases more and more, the current flow formed at the channel of the first PMOS transistor 46 of the voltage sharing
25 circuit 80 is reduced more and more, so that the internal supply voltage of the output node 49 of the output circuit 70 increases with reference to increase of the temperature. As a result, since the deterioration of MOS transistor due to

variation of the temperature is prevented, it can be possible to cause an associated semiconductor memory device driven by the voltage $V_{cc_{int}}$ to operate stably.

5 For a better understanding of the voltage sharing circuit 80 of Figure 6, the table in Figure 7 will be described hereinbelow, wherein the current driving power decrease ratio is shown in detail for MOS transistors with the gate oxide layer thereof being $160\text{\AA}$ thick. In the following, as a matter of convenience, a PMOS transistor will be described together with an NMOS
10 transistor; however, the matters related to the PMOS transistor are described in parenthesis. In the table, the current driving power for the NMOS (PMOS) transistor is measured under the condition that the gate and drain voltages applied thereto are both $+4.0\text{V}$ (-4.0V), and the substrate-source voltage is -2.0V (0V). The current driving power decrease ratio at 85°C is illustrated in
15 comparison with the current driving power decrease ratio at 25°C . It will be understood to a person skilled in the art that a high decrease ratio of the current driving power means a high increase ratio of the channel resistance in response to increase of the temperature, of the MOS transistor. Accordingly, as the channel conductance of the MOS transistor is made low, the channel
20 resistance thereof is high and, thus, the resistance increase ratio thereof is also high.

From the foregoing descriptions, it may be understood that an internal supply voltage generator of Figure 4 and/or 6 can compensate for a decrease
25 of current driving power due to increase of temperature as well as for decrease of operational speed due to decrease of current driving power. Therefore, a

semiconductor memory device employing such a circuit may be operated stably regardless of the variation of the temperature.

5 Although specific constructions and procedures of the invention have been illustrated and described herein, it is not intended that the invention be limited to the elements and constructions disclosed. One skilled in the art will easily recognize that the particular elements or subconstructions may be used without departing from the scope of the invention.

10 It will be understood by those skilled in the art that, in the context of this specification, the term "ground level" may include reference potentials other than 0_v.

CLAIMS

1. A circuit for receiving an external supply voltage and for generating an internal supply voltage lower than said external supply voltage, for use in a semiconductor memory device, the circuit comprising:

5 a reference voltage generating means connected to receive said external voltage, for generating a reference voltage;

a comparator means connected to receive the output of said reference voltage generating means, for comparing a signal applied from a first
10 input line with a signal from a second input line, the first input line being coupled to the output of said reference voltage generating means;

an output means receiving the output of said comparator means, for generating at an output node thereof said internal supply voltage; and

15 a voltage sharing means for receiving the output of said output means, and supplying an output to the second input line of said comparator means:

wherein the output of said output means has a tendency to increase in
20 response to increase of the temperature, thus compensating for a decrease in the reference voltage caused by the increase in temperature, to provide an output which is substantially independent of temperature.

2. A circuit as claimed in Claim 1, wherein said reference voltage generating
25 means comprises:



a first resistor one end thereof being connected to an output node of said reference voltage generator;

5 a first bipolar transistor of which a collector and base are commonly coupled to the other end of said first resistor and of which an emitter is coupled to a ground level;

10 a second resistor one end thereof being connected to the output node of said reference voltage generator;

a second bipolar transistor of which a collector is coupled to the other end of said second resistor and of which a base is coupled to the collector of said first bipolar transistor;

15 a third resistor, one end thereof being coupled to an emitter of said second bipolar transistor, the other end thereof being coupled to said ground level; and

20 a third bipolar transistor of which a collector is coupled to the output node of said reference voltage generator, and of which a base is coupled to the collector of said second bipolar transistor, of which the emitter is coupled to said ground level.

25 3. A circuit as claimed in Claim 1 or 2, wherein said comparator means comprises:



a first PMOS transistor of which a source is coupled to said external supply voltage;

5 a second PMOS transistor of which a source is coupled to said external supply voltage and of which a gate and drain are commonly coupled to a gate of said first PMOS transistor;

10 a first NMOS transistor of which a gate is coupled to the first input line and of which a drain is coupled to a drain of said first PMOS transistor;

a second NMOS transistor of which a gate is coupled to the second input line, and of which a drain is coupled to the drain of said second PMOS transistor;

15 a third NMOS transistor of which a gate is coupled to the first input line, a source is coupled to said ground level, and of which a drain is coupled to sources of the first and second NMOS transistors; and

20 an output node formed at a connection of the drains of the first PMOS transistor and the first NMOS transistor.

4. A circuit as claimed in any one of claims 1 to 3, wherein said output means comprises:

25 a PMOS transistor of which a source is coupled to the external supply voltage, and of which a gate is coupled to the output node of said comparator means; and



an output node coupled to a drain of said PMOS transistor.

5. A circuit according to any one of claims 1 to 4, wherein said voltage sharing means tends to increase said internal supply voltage in response to increase of temperature, said voltage sharing means comprising:

first and second variable resistor means coupled in series between said output means and a ground level, and having

- an output node formed at a connection of said first and second variable resistor means.

6. A circuit as claimed in Claim 5, wherein a resistance increase ratio in response to increase of the temperature, of said first variable resistor means, is higher than that of said second variable resistor means.

7. A circuit as claimed in Claim 5 or 6, wherein said first and second variable resistor means comprises:

- a first MOS transistor having an end of a channel thereof coupled to said output means, and another end of the channel and a gate thereof being diode-connected; and

- a second MOS transistor having an end of a channel thereof coupled to said output node, and another end of the channel and a gate thereof being diode-connected to said ground level:



said first MOS transistor having a channel longer in length than that of said second MOS transistor.

8. A circuit as claimed in any one of claims 1 to 4, wherein said voltage
5 sharing means comprises:

a first PMOS transistor of which a source is coupled to the output node of said output means, and of which a gate and drain are diode-connected;

10 a second PMOS transistor of which a source is coupled to the drain of said first PMOS transistor, and of which a gate and drain are diode-connected to said ground level; and

15 an output node formed at a common connection of the first and second PMOS transistors.

9. A circuit substantially as hereinbefore described with reference to Figure 4, or with reference to Figure 4 together with Figure 5 and/or Figure 6, of the accompanying drawings.

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10. A semiconductor memory device provided with a circuit according to any of the preceding claims.

