CLAIMS

1. A semiconductor device comprising:

a first insulating layer;

a first oxide insulating layer over the first insulating layer;

an oxide semiconductor layer over the first oxide insulating layer;

a source electrode layer and a drain electrode layer over the oxide semiconductor layer;

a second insulating layer over the first insulating layer, the source electrode layer, the drain electrode layer, and the oxide semiconductor layer;

a second oxide insulating layer over the oxide semiconductor layer;

a gate insulating layer over the second oxide insulating layer;

a gate electrode layer over the gate insulating layer; and

a third insulating layer over the second insulating layer, the second oxide insulating layer, the gate insulating layer, and the gate electrode layer,

wherein a side surface portion of the second insulating layer is in contact with the second oxide insulating layer,

wherein the gate electrode layer includes a first region, a second region, and a third region that have different widths,

wherein the first region is located over the second region,

wherein the second region is located over the third region,

wherein the third region has a width larger than that in a lower portion of the second region, and

wherein top surfaces of the gate insulating layer, the gate electrode, and the second insulating layer are coplanar.

2. The semiconductor device according to claim 1,

wherein in the gate electrode layer, a side surface portion of the gate electrode layer includes at least one inflection point in a cross section parallel to a thickness direction of the gate electrode layer.

3. The semiconductor device according to claim 1,

wherein in the gate electrode layer, a side surface portion of the first region extends beyond a tangent of a side surface portion of the second region.

4. The semiconductor device according to claim 1,

wherein a side surface portion of the gate electrode layer includes two or more taper angles.

5. A semiconductor device comprising:

a first insulating layer;

a first oxide insulating layer over the first insulating layer;

an oxide semiconductor layer over the first oxide insulating layer;

a source electrode layer and a drain electrode layer over the oxide semiconductor layer;

a second insulating layer over the first insulating layer, the source electrode layer, the drain electrode layer, and the oxide semiconductor layer;

a second oxide insulating layer over the oxide semiconductor layer;

a gate insulating layer over the second oxide insulating layer;

a gate electrode layer over the gate insulating layer; and

a third insulating layer over the second insulating layer, the second oxide insulating layer, the gate insulating layer, and the gate electrode layer,

wherein a side surface portion of the second insulating layer is in contact with the second oxide insulating layer,

wherein the gate electrode layer includes a first region, a second region, and a third region that have different widths,

wherein the first region is located over the second region,

wherein the second region is located over the third region,

wherein the third region has a width larger than that in a lower portion of the second region, and

wherein top surfaces of the gate insulating layer, the gate electrode, and the second insulating layer are coplanar.

6. The semiconductor device according to claim 5,

wherein a side surface portion of the first region or the third region of the gate electrode layer extends beyond a tangent formed in the second region of the gate electrode layer.

7. The semiconductor device according to claim 5,

wherein a side surface portion of the gate electrode layer includes two or more inflection points in a cross section parallel to a thickness direction of the gate electrode layer.

8. The semiconductor device according to claim 5,

wherein a side surface portion of the gate electrode layer includes three or more taper angles.

9. A semiconductor device comprising: an oxide semiconductor layer;

a source electrode layer and a drain electrode layer over the oxide semiconductor layer;

an insulating layer over the source electrode layer and the drain electrode layer,

the insulating layer including a groove;

a gate insulating layer over the oxide semiconductor layer; and

a gate electrode layer over the gate insulating layer,

wherein the gate electrode layer is in the groove,

wherein the gate electrode layer includes a first region and a second region,

wherein the first region is over the second region, and

wherein the second region has a width larger than that in a lower portion of the first region.

10. The semiconductor device according to claim 9,

wherein in the gate electrode layer, a side surface portion of the gate electrode layer includes at least one inflection point in a cross section parallel to a thickness direction of the gate electrode layer.

11. The semiconductor device according to claim 9,

wherein in the gate electrode layer, a side surface portion of the first region extends beyond a tangent of a side surface portion of the second region.

12. The semiconductor device according to claim 9,

wherein a side surface portion of the gate electrode layer includes two or more taper angles.