

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICESAND A PROCESS FOR PRODUCING THE SAME

The present invention relates to semiconductor integrated circuit devices and a process for producing the same.

In semiconductor integrated circuit devices, and particularly in semiconductor integrated circuit devices containing a plurality of metal oxide film semiconductor-type field effect transistors (hereinafter referred to as MISFET's), the wiring layer has often been made of polycrystalline silicon which has resistance against heat and self-aligning properties, instead of aluminum. The polycrystalline silicon is doped with impurities in order to reduce its very great resistivity. Even after doping with impurities, however, the polycrystalline silicon still exhibits great resistivity compared with aluminum. In the semiconductor integrated circuit devices employing polycrystalline silicon as a wiring layer, therefore, the defect is that the signals are transmitted at slow speeds.

In order to preclude the above-mentioned defect, therefore, it has been known to use a refractory metal such as molybdenum, tungsten, platinum, or tantalum as a material for forming wiring layers (Japanese Patent

Laid-Open No. 80986/1978). When a refractory metal is used in pure form as a material for forming wiring layers in the semiconductor integrated circuit device, the device will exhibit small resistivity and increased resistance against the heat treatment, but will present defects such as poor adhesiveness of the layer to the SiO_2 film or Si_3N_4 film.

Therefore, it has been attempted to use a silicide layer composed of silicon and a refractory metal as a wiring layer for the semiconductor integrated circuit devices (Japanese Patent Laid-Open No. 80986/1978). This wiring layer, however, cannot be intimately adhered onto the SiO_2 film, and does not provide good contacting property to the silicon substrate, either.

In order to eliminate the above-mentioned defects, furthermore, an attempt has been made to use a wiring layer with double-layer construction consisting of a polycrystalline silicon layer and a silicide layer of silicon and a refractory metal formed on the polycrystalline silicon layer (Japanese Patent Laid-Open No. 88783/1979). Here, however, the wiring layer with the double-layer construction has a resistivity which is considerably greater than that of a pure refractory metal though it varies depending upon the silicon content in the silicide layer. For example, when molybdenum is used as the refractory metal,

the wiring layer consisting of a polycrystalline silicon layer and a silicide layer of silicon and molybdenum formed on the polycrystalline silicon layer, exhibits a resistivity of 100 to 150 x 10⁻⁶ ohms.cm in contrast
5 with the resistivity of pure molybdenum of about 15 x 10⁻⁶ ohms.cm.

According to a first aspect of the present invention there is provided a semiconductor memory integrated circuit device comprising data lines extending in parallel with
10 each other, word lines extending in a direction generally at right angles to said data lines, and memory cells coupled between said data lines and said word lines, wherein each of said word lines comprises three successive layers of a polycrystalline silicon layer, a refractory
15 metal silicide layer formed on said polycrystalline silicon layer, and a refractory metal layer formed on said refractory metal silicide layer.

According to a second aspect of the present invention there is provided a semiconductor integrated circuit
20 device comprising a semiconductor substrate having one main surface, an insulating film formed on said main surface of said semiconductor substrate, said insulation film having a hole exposing a portion of said main surface, a semiconductor region of one conductivity type formed at an
25 area including said exposed portion in said semiconductor substrate, and a conductive layer in contact with said semiconductor region at said exposed portion and extending over said insulating film, wherein said conductive layer

comprises three successive layers of a polycrystalline silicon layer in contact with said semiconductor region at said exposed region and extending on said insulating film, a refractory metal silicide layer, and a refractory metal layer, said polycrystalline silicon layer being
5 doped with impurities of the same conductivity as that of said semiconductor region.

According to a third aspect of the present invention there is provided a semiconductor integrated circuit device
10 comprising an insulating film formed on one main surface of a semiconductor substrate, said insulating film including a thick field insulating film and a thin gate insulating film, a gate electrode strip selectively formed on said gate insulating film and extending on said field
15 insulating film, source and drain regions formed in said semiconductor substrate on both sides of said gate electrode strip, and a wiring strip contacting at least one of the source and drain regions and extending on said field insulating film, wherein the gate electrode strip and the
20 wiring strip each comprise three successive layers of a polycrystalline silicon layer, a refractory metal silicide layer formed on said polycrystalline silicon layer, and a refractory metal layer formed on said refractory metal silicide layer.

25 According to a fourth aspect of the present invention there is provided a MIS-type field effect transistor comprising a gate insulating film formed on one main surface of a semiconductor substrate, a gate electrode selectively

formed on said gate insulating film, said gate electrode having two sides, source and drain respectively regions formed in the semiconductor substrate on the two sides of said gate electrode, and a contacting electrode which is

5 contacted with at least one of said source and drain regions, wherein said gate electrode comprises three successive layers of a polycrystalline silicon layer formed on said gate insulating film, a refractory metal silicide layer formed on said polycrystalline silicon layer, and a

10 refractory metal layer formed on said refractory metal silicide layer, and wherein said source and drain regions are aligned with respective opposite edge portions of said gate electrode, and said contacting electrode comprises three successive layers of a polycrystalline silicon layer

15 contacted with at least one of said source and drain regions, a refractory metal silicide layer for the contact electrode which is formed on said polycrystalline silicon layer and in contact with at least one of said source and drain regions, and a refractory metal layer on said

20 refractory metal silicide layer for the contact electrode.

According to a fifth aspect of the present invention there is provided a process for producing semiconductor devices including the following steps:

- (a) forming an insulating film on one main surface
- 25 of a semiconductor substrate;
- (b) forming a polycrystalline silicon layer on said insulating film;

(c) forming a deposited layer of silicon and a refractory metal by simultaneously sputtering silicon and a refractory metal on said polycrystalline silicon layer;

(d) forming a refractory metal layer on the deposited
5 layer of silicon and the refractory metal; and

(e) annealing said polycrystalline silicon layer, said deposited layer and said refractory metal layer.

According to a sixth aspect of the present invention there is provided a process for producing semiconductor
10 devices by forming an insulating film on one main surface of a semiconductor substrate, and by selectively forming a gate electrode on the insulating film, wherein said gate electrode is formed by the following procedure: a polycrystalline silicon layer is formed by the CVD method
15 on said insulating film, silicon and a refractory metal are deposited on said polycrystalline silicon layer by the co-sputtering method, a refractory metal layer is formed on the deposited layer by sputtering, and the polycrystalline silicon layer, the deposited layer and the refractory metal
20 layer are selectively removed and annealed.

Fig. 1 is a section of a semiconductor integrated circuit device according to an embodiment of the present invention;

Fig. 2 is a circuit diagram of a D-RAM according to
25 the present invention;

Fig. 3 is a diagram of the lay-out pattern of a D-RAM IC of the two-mat system according to the present invention;

Fig. 4 is a perspective sectional view showing the construction of memory cell elements according to the present invention;

5 Fig. 5 is a perspective sectional view showing the construction of dummy cell elements according to the present

invention;

Fig. 6 is a perspective sectional view showing a portion of the elements in an active restore circuit according to the present invention;

5 Fig. 7 is a diagram of the lay-out pattern of a memory array and a dummy array according to the present invention;

Fig. 8 is a plan view showing a portion of a semiconductor substrate which illustrates the state of a field insulation film according to the present invention;

10 Fig. 9 is a plan view showing a portion of a semiconductor substrate which illustrates the state of a first conductor layer according to the present invention;

Fig. 10 is a plan view of a semiconductor integrated circuit device which constitutes the active restore circuit according to the present invention; and

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Figs. 11A to 11S are sectional views of the semiconductor integrated circuit device in each of the steps for producing the D-RAM according to the present invention.

20 DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will be described below with reference to an embodiment.

Fig. 1 is a section view of an MIS-type semiconductor integrated circuit device according to an embodiment of the present invention, in which reference numeral 51 denotes

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a p-type silicon substrate, and 52 denotes a field insulating film which is selectively formed by thermal oxidation. An MISFET is formed in a region surrounded by the field insulating film 52. The MISFET consists of a gate insulating film 53 formed by surface oxidation; a gate electrode of a three-layer construction which is made up of a polycrystalline silicon layer 542, a silicide layer (hereinafter referred to as molybdenum silicide layer) 552 of silicon and molybdenum, and a pure molybdenum layer 562; and an N^+ -type semiconductor region 572 which is formed using the gate electrode as a mask and which serves as a self-aligned source region or a drain region; and an N^+ -type semiconductor region 573.

The N^+ -type semiconductor region 572 is connected to other MISFETs through a wiring layer of a three-layer construction consisting of a polycrystalline silicon layer 541, a silicide layer (hereinafter referred to as molybdenum silicide layer 551) of silicon and molybdenum, and a pure molybdenum layer 561, which is in direct contact with an N^+ -type semiconductor region 571 that is continuous with the N^+ -type semiconductor region 572. Further, the N^+ -type semiconductor region 573 is connected to other MISFETs through an aluminum layer 60.

The above gate electrode works not simply as a gate for the MISFET but also as a wiring layer for connecting

the gate electrode to, for example, the gates of other MISFET's in the semiconductor integrated circuit device.

— As mentioned already, the time required for transmitting the signals through the wiring layer in the semiconductor integrated circuit should be as short as possible and, for this purpose, the resistivity should be as small as possible. In a dynamic random access memory, in particular, it is desired to reduce the resistivity of the wiring layer as far as possible to increase the speed of transmission of the signals.

The wiring layer of the three-layer construction consisting of a polycrystalline silicon layer, a molybdenum silicide layer and a pure molybdenum layer, exhibits a resistivity of about 30 to 35 microohms-cm. This is about twice that of pure molybdenum which has a resistivity of about 15 microohms-cm, and is about one-fifth to one-third that of the conventional wiring layer which wholly or partly consists of a refractory metal.

The reason why such a small resistivity can be realized is attributed to the presence of the layer of pure molybdenum which forms the uppermost layer of the wiring layer. According to the study conducted by the inventors of the present invention, it was clarified

that even when a heat treatment is performed during or after the wiring layer is formed, the three layers constituting the wiring layer do not react among themselves, but retain their properties. Moreover, the polycrystalline silicon layer which forms the lowermost layer of the wiring layer adheres intimately to an insulating film such as SiO_2 film, Si_3N_4 film, or the like, and also comes into ohmic contact with the silicon substrate.

The wiring layer of the three-layer construction of the present invention shown in Fig. 1, can be obtained as mentioned below. The polycrystalline silicon layers 541, 542 is formed over the whole surface by the vapor-phase chemical reaction method (CVD method) to a thickness of about 1500 to 2500 angstroms, and is doped with phosphorus ions to a high concentration to reduce the resistivity. Thereafter, molybdenum silicide layer 551, 552 is formed over the whole surface of the polycrystalline silicon layer by, for example, co-sputtering to a thickness of about 1000 angstroms. The silicon content will be 10 % by weight. Then, pure molybdenum layer 561, 562 is formed on the whole surface of the molybdenum silicide layer by, for example, the sputtering method to a thickness of about 1500 angstroms. Using $\text{CF}_4 + \text{O}_2$ gas, the above-mentioned layers are continuously subjected to plasma etching to form a wiring layer of the three-layer

construction having a predetermined shape as shown in Fig. 1.

Thereafter, the wiring layer is annealed in a nitrogen atmosphere such that the uppermost molybdenum layers 561, 562 will not be oxidized or sublimated. The annealing is effected in order that silicon is uniformly dispersed in the molybdenum layers 551, 552 which contain silicon.

In performing the annealing, it was found that the above-mentioned three layers cease to exist if the silicon is contained in a stoichiometric amount, i.e., when the silicon content is 37 % by weight. Namely, when the silicon is contained in a stoichiometric amount, the individual layers undergo chemical reaction, and the stress resulting from the contraction of volume causes the individual layers to be peeled off from each other.

With the present method, however, the above-mentioned three layers are bonded to each other, and the resistivity of the wiring layer can be reduced to a value as small as 30 to 35 microhms·cm.

Furthermore, the following effects can be obtained:

(1) It is possible to prevent the formation of SiO_2 film on the interface between the polycrystalline silicon layers 541, 542 and the molybdenum silicide layers 551, 552. The

molybdenum silicide layers 551, 552 are formed by co-sputtering. In this case, oxygen in the atmosphere is taken into the molybdenum silicide layers 551, 552.

Prior to reacting with silicon in the polycrystalline silicon layers 541, 542, the oxygen reacts with silicon contained in the molybdenum silicide layers 551, 552 to form SiO_2 . Therefore, no SiO_2 film is formed on the interface. Further, since silicon is present in an isolated manner in the molybdenum silicide layers 551, 552, the SiO_2 film is not formed in a continuous manner. Further, the oxygen in the atmosphere is taken into the molybdenum layers 561, 562 when they are being formed by the sputtering. The oxygen reacts with silicon in the molybdenum silicide layers 551, 552. However, since silicon is present in an isolated manner, oxide film is not formed continuously on the interface.

Since no oxide film is formed on the interface, the resistivity of the wiring layer does not increase.

It was found through the study conducted by the inventors of the present invention that a substance that serves as an oxygen getter should be contained in the second layer so that oxygen taken from the atmosphere will not form an oxide film on the interface. It was confirmed that such a substance needs be contained in an amount of 5 % by weight to 10 % by weight. The substance which

serves as an oxygen getter should be determined by taking into consideration the chemical relation to the three layers forming the wiring layer, i.e., by taking into consideration the adhesiveness and the chemical reaction that may take place during the step of heat treatment.

(2) When the wiring layer consisting of the polycrystalline silicon layer 541, the molybdenum silicide layer 551 formed thereon, and the molybdenum layer 561, is brought into direct contact with the semiconductor region to form an electrode, the resulting ohmic contact obviates the need for forming a high-concentration region. This is due to the fact that impurities doped in the polycrystalline silicon are diffused into the semiconductor region to form a high-concentration region.

(3) Impurities are taken from the atmosphere into the molybdenum silicide layers 551, 552 when they are formed by the co-sputtering. However, since there exists a polycrystalline silicon layer therebetween, impurities such as sodium ions are not diffused into the activated semiconductor region.

As described above, therefore, it is possible to obtain a semiconductor integrated circuit device having a small resistivity and a short signal transmission time.

The invention will be described below by way of concrete embodiments. In the below-mentioned embodiments, the present invention is adapted to a dynamic random access memory (hereinafter referred to as D-RAM).

5 First, the setup of the D-RAM circuit is briefly mentioned below with reference to Fig. 2.

The D-RAM circuit consists of an address buffer ADB for introducing address signals $A_0 - A_j$, a row and column decoder RC-DCR for selecting a given row address line and a given column address line from the row address signals
10 $A_0 - A_i$ and the column address signals $A_{i+1} - A_j$, a memory array M-ARY having a plurality of memory cells M-CEL's, a dummy array D-ARY having a plurality of dummy cells D-CEL's, a column switch C-SW₁ for selecting any data line in the
15 M-ARY responsive to a selected column address signal, a sense amplifier SA, a data input buffer DIB, an output amplifier OA, and a data output buffer DOB.

The M-CEL consists of a capacitor C_s for storing the data and an MISFET Q_M for selecting the address, and the
20 data "1" or "0" is stored in the form of whether there is electric charge in the capacitor C_s or not.

The D-RAM circuit is arrayed on a single semiconductor chip as concretely shown in Fig. 3.

Fig. 3 is a diagram of lay-out pattern of the D-RAM IC
25 of a so-called two-mat system in which the memory array

is divided into two in a single semiconductor chip.

First, the two memory arrays $M-ARY_1$ and $M-ARY_2$ consisting of a plurality of memory cells are placed in an IC chip, separated away from each other.

5 A common column decoder C-DCR is arrayed on the central portion of the IC chip between $M-ARY_1$ and $M-ARY_2$.

The column switch $C-SW_1$ for the $M-ARY_1$ and the dummy array $D-ARY_1$ consisting of a plurality of dummy cells are placed between $M-ARY_1$ and C-DCR.

10 On the other hand, the column switch $C-SW_2$ for the $M-ARY_2$ and the dummy array $D-ARY_2$ consisting of a plurality of dummy cells are placed between $M-ARY_2$ and C-DCR.

The sense amplifiers SA_1 and SA_2 are located at an extreme left portion and at an extreme right portion of the
15 IC chip, so that they will not be erroneously operated by noise such as signals applied to the C-DCR, and so that the wiring can be easily laid out.

On the upper left side of the IC chip are arrayed a data input buffer DIB, a read and write control signal
20 generator R/W-SG, a RAS signal generator RAS-SG, and a RAS family signal generator SG_1 . Adjacent to these circuits, there are further arrayed a $\overline{RAS}$ signal applying pad $P-\overline{RAS}$, a $\overline{WE}$ signal applying pad $P-\overline{WE}$, and a data signal applying pad $P-D_{in}$.

25 On the upper right side of the IC chip, on the other

hand, there are arrayed a data output buffer DOB, a CAS signal generator CAS-SG, and a CAS family signal generator SG₂. Adjacent to these circuits, there are arrayed a V_{ss} voltage supplying pad P-V_{ss}, a $\overline{\text{CAS}}$ signal applying pad P- $\overline{\text{CAS}}$, a data signal output pad P-D_{out}, and an address signal A₆ supplying pad P-A₆.

A main amplifier MA is placed between the RAS family signal generator SG₁ and the CAS family signal generator SG₂.

10 A V_{BB} generator V_{BB}-G is located above a circuit which occupies large areas such as RAS family signal generator SG₁, CAS family signal generator SG₂ or main amplifier MA. This is because, the V_{BB}-G produces a minority carrier, and the data in the memory cells constituting the M-ARY₁ and M-ARY₂ may be undesirably inverted by the minority carriers. In order to prevent such a probability, therefore, the V_{BB} generator V_{BB}-G is located at a position remote from the M-ARY₁ and M-ARY₂.

20 The row decoder R-DCR₁ for the M-ARY₁ is located on the lower left side of the IC chip. Adjacent to the R-DCR₁, there are arrayed address signal supplying pads P-A₀, P-A₁, P-A₂, and a V_{CC} voltage supplying pad P-V_{CC}.

On the lower right side of the IC chip, on the other hand, there is provided a row decoder R-DCR₂ for the M-ARY₂. Adjacent to the row decoder R-DCR₂, there are arrayed address

signal applying pads $P-A_3$, $P-A_4$, $P-A_5$, and $P-A_7$.

An address buffer ADB is disposed between $R-DCR_1$ and $R-DCR_2$.

5 The D-RAM IC has a capacity of about 64 kilobits divided into two memory cell matrixes (memory arrays $M-ARY_1$ and $M-ARY_2$) each having a memory capacity of 128 rows x 256 columns = 32,768 bits (32 kilobits). Therefore, one memory array has 128 word lines WL and 256 data lines DL.

10 The above data lines DL are made of aluminum and have a small resistivity. Further, as will be obvious from Fig. 3, the data lines DL are short and impose no problem with regard to the time for transmitting the signals applied by the column decoder C-DCR to each of the memory
15 cells.

On the other hand, as will be understood from Fig. 3, the word lines WL are much longer than the data lines DL. If the word lines WL have large resistivities, extended periods of time are needed to transmit the signals applied
20 by the row decoder R-DCR to each of the memory cells, particularly to transmit the signals applied by the row decoder R-DCR to the memory cells located at the most remote positions.

The signal transmission time of the word lines WL
25 determines the operation time of the D-RAM, and eventually

determines the operation time of the whole D-RAM system.

According to the embodiment of the present invention, the word lines WL consist of a polycrystalline silicon layer, a molybdenum silicide layer formed thereon, and a
5 pure molybdenum layer formed further thereon, as shown in Fig. 1. The word lines have a resistivity of 30 to 35 microohms·cm which is one-fifth to one-third that of the conventional word lines. According to the embodiment of the present invention, therefore, the D-RAM permits the
10 signals to transmit in less time than the conventional D-RAM, and operates at speeds faster than the conventional D-RAM. Further, the whole D-RAM system can be operated at high speeds.

According to the embodiment of the present invention,
15 furthermore, not only the word lines but also the gate electrodes of all MISFET's in the D-RAM are formed in the three-layer construction. Accordingly, the D-RAM operates at higher speeds.

Construction of the principal elements and lay-out
20 pattern in the embodiment of the present invention will be discussed below in further detail.

[Construction of memory cell M-CEL]

Fig. 4 is a perspective section view showing the construction of a memory cell M-CEL of Fig. 2, in which
25 reference numeral 1 denotes a p-type semiconductor

substrate, 2 denotes a relatively thick insulating film (hereinafter referred to as field insulating film), 3 denotes a relatively thin insulating film (hereinafter referred to as gate insulating film), 4 and 5 denote N^+ -type semiconductor regions, 6 denotes a first polycrystalline silicon layer, 7 denotes an n-type surface inverter layer, 8 denotes a second polycrystalline silicon layer, 9 denotes a PSG (phosphorus silicate glass) layer, 10 denotes an aluminum layer, 29 denotes a molybdenum silicate layer, and 36 denotes a molybdenum layer.

A MISFET Q_M in a memory cell M-CEL has a substrate, a source region, a drain region, a gate insulating film and a gate electrode, that are, respectively, made up of the above-mentioned p-type semiconductor substrate 1, the n^+ -type semiconductor region 4, the n^+ -type semiconductor region 5, the gate insulating film 3, and a multi-layer electrode consisting of a second polycrystalline silicon layer 8, a molybdenum silicide layer 29, and a molybdenum layer 36. The multi-layer electrode can be used, for example, as a word line WL_{1-2} which is shown in Fig. 2. The aluminum layer 10 connected to the n^+ -type semiconductor region 5 is used, for example, as a data line DL_{1-1} which is shown in Fig. 2.

On the other hand, a memory capacitor C_s in the memory cell M-CEL has an electrode, a dielectric layer and another

electrode which are, respectively, made up of a first polycrystalline silicon layer 6, a gate insulating film 3, and an n-type surface inverted layer 7. Namely, the power-supply voltage V_{CC} applied to the first polycrystalline silicon layer 6 induces the n-type surface inverted layer 7 on the surface of the p-type semiconductor substrate 1 through the gate insulating film 3 owing to the effect of the electric field.

[Construction of dummy cell D-CEL]

Fig. 5 is a perspective section view showing the construction of a dummy cell D-CEL which is illustrated in Fig. 2. In Fig. 5, reference numerals 11 to 14 denote n⁺-type semiconductor regions, 15 denotes a first polycrystalline silicon layer, 16 denotes an n-type surface inverted layer, 17 and 18 denote second polycrystalline silicon layers, 19 denotes an aluminum layer, 30 and 31 denote molybdenum silicide layers, and 37 and 38 denote molybdenum layers.

A MISFET Q_{D1} in a dummy cell D-CEL has a substrate, a drain region, a source region, a gate insulation film and a gate electrode, which are, respectively, made up of the p-type semiconductor substrate, an n⁺-type semiconductor region 11, an n⁺-type semiconductor region 12, a gate insulating film 3, and a multi-layer electrode consisting of a second polycrystalline silicon layer 17, a

molybdenum silicide layer 30 and a molybdenum layer 37.

The multi-layer electrode stretches on the p-type

semiconductor substrate 1 as a dummy word line DWL_{1-2}

which is shown in Fig. 2. The aluminum layer 19 connected

5 to the n^+ -type semiconductor region stretches on the p-type semiconductor substrate 1 as a dummy data line $\overline{DL}_{1-1}$ shown in Fig. 2.

A MISFETQ_{D2} in the dummy cell D-CEL has a substrate,

a drain region, a source region, a gate insulating film

10 and a gate electrode, that are, respectively, made up

of the p-type semiconductor substrate 1, an n^+ -type semi-

conductor region 13, an n^+ -type semiconductor region 14,

a gate insulating film 3, and a multi-layer electrode

consisting of a second polycrystalline silicon layer 18, a

15 molybdenum silicide layer 31 and a molybdenum layer 38.

The multi-layer electrode is served with a discharge signal

ϕ_{dc} which is diagrammed in the dummy cell D-CEL of Fig. 2.

The capacitor C_{ds} in the dummy cell D-CEL has one elec-

trode, a dielectric layer and another electrode, that are,

20 respectively, made up of a first polycrystalline silicon

layer 15, a gate insulating film 3 and an n-type surface

inverted layer 16. Namely, the power-supply voltage V_{CC}

applied to the first polycrystalline silicon layer 15

induces the n-type surface inverted layer 16 on the

25 surface of the p-type semiconductor substrate 1 via the

gate insulating film 3 owing to the effect of the electric field.

[Construction of a portion of a peripheral circuit (active restore AR_1)]

5 Fig. 6 is a perspective section view showing the construction of a portion of the peripheral circuit formed in the periphery of the memory array M-ARY, i.e., showing a portion of the active restore AR_1 which is shown in Fig. 2. In Fig. 6, reference numerals 20 to 23 denote n^+ -
10 type semiconductor regions, 24 to 27 denote second polycrystalline silicon layers, and 28 denotes an aluminum layer. Reference numerals 32 to 35 denote molybdenum silicide layers, and 39 to 42 denote molybdenum layers.

15 A MISFET Q_{36} in the active restore AR_1 shown in Fig. 2 has a substrate, a source region, a drain region, a gate insulating film and a gate electrode, that are, respectively, made up of a p-type semiconductor substrate 1, an n^+ -type semiconductor region 20, an n^+ -type semiconductor region
20 21, a gate insulating film 3, and a multi-layer electrode consisting of a second polycrystalline silicon layer 24, a molybdenum silicide layer 32 and a molybdenum layer 39.

 A MISFET Q_{34} in the active restore AR_1 has a substrate, a source region, a drain region, a gate insulating film and
25 a gate electrode, that are, respectively, made up of a p-type

semiconductor substrate 1, an n^+ -type semiconductor region 22, an n^+ -type semiconductor region 23, a gate insulating film 3, and a multi-layer electrode consisting of a second polycrystalline silicon layer 27, a molybdenum silicide layer 35 and a molybdenum layer 42. The multi-layer electrode is served with an active restore control signal ϕ_{rg} which is shown in Fig. 2.

A capacitor C_{B11} in the active restore AR_1 has a dielectric layer and an electrode that are, respectively, made up of the gate insulating film 3 and a multi-layer electrode consisting of a second polycrystalline silicon layer 25, a molybdenum silicide layer 33 and a molybdenum layer 40. The multi-layer electrode is connected to a multi-layer electrode which serves as a gate electrode of the MISFETQ_{S6} and which consists of a second polycrystalline silicon layer 24, a molybdenum silicide layer 32 and a molybdenum layer 39. Further, a portion 25a of the second polycrystalline silicon layer 25 is directly connected to the n^+ -type semiconductor region 22 of the MISFETQ_{S4}. This is because, if the molybdenum layer 40 and the n^+ -type semiconductor region 22 are connected together via an aluminum wiring layer, a contact area must be formed between the molybdenum layer 40 and the aluminum wiring layer and makes it difficult to increase the wiring density. Therefore, the above-mentioned connection means

is employed to increase the wiring density.

Another electrode of the capacitor C_{B11} consists of an inverted layer which is formed on the surface of the semiconductor substrate 1. The inverted layer is established by a voltage which is applied to the multi-layer electrode consisting of the second polycrystalline silicon layer 25, a molybdenum silicide layer 33 and a molybdenum layer 40. Although not diagrammed in Fig. 6, the inverted layer is contiguous with the n^+ -type semiconductor region which is formed in the semiconductor substrate 1 and which is served with an active restore control signal ϕ_{rs} of Fig. 2. Further, as an electrode of the capacitor C_{B11} , there may exist a molybdenum silicide layer and a molybdenum layer on the polycrystalline silicon layer.

The multi-layer electrode consisting of a second polycrystalline silicon layer 26, a molybdenum silicide layer 34 and a molybdenum layer 41, serves as one electrode of the capacitor C_{B12} which is shown in Fig. 2, and a portion thereof is directly connected to the source region of the MISFETQ_{S5} of Fig. 2 like the capacitor C_{B11} , and another portion thereof is connected to the gate electrode of the MISFETQ_{S7}.

[Lay-out patterns of memory array M-ART and dummy array D-ARY]

Lay-out patterns of the aforementioned memory array M-ARY and the dummy array D-ARY are described below with reference to Fig. 7.

The memory array M-ARY shown in Fig. 7 has a plurality of memory cells M-CEL shown in Fig. 4, which are arrayed on the semiconductor substrate 1. On the other hand, the dummy array D-ARY shown in Fig. 7 has a plurality of dummy cells D-CEL of Fig. 5, which are arrayed on the semiconductor substrate 1.

First, the memory array M-ARY shown in Fig. 7 is constructed as mentioned below.

The field insulating film 2 is formed describing a pattern as shown in Fig. 8 in order to separate a plurality of memory cells M-CEL which are composed of MISFETs Q_M and memory capacitors C_S on the surface of the semiconductor substrate 1.

Exceptionally, however, in the present embodiment a field insulating film 2a is formed beneath the contact holes CH_0 through which the power-supply voltage V_{CC} is applied to the first polycrystalline silicon layer 6. This is different from the general rule of such layouts. Therefore, no aluminium-silicon alloy formed by the reaction between the aluminum layer and the polycrystalline silicon layer in the vicinity of the contact holes CH_0 is allowed to penetrate through the

insulation film beneath the contact holes CH_0 , and is prevented from reaching the surface of the semiconductor substrate 1.

5 The first polycrystalline silicon layer 6 which serves as one electrode of the memory capacitor C_s in the memory cells M-CEL is formed on the field insulating film 2 and on the gate insulating film 3 describing a pattern as shown in Fig. 9.

10 Further, word lines WL_{1-1} composed of multi-layer wiring of the second polycrystalline silicon layer 8, the molybdenum silicide layer 29 and the molybdenum layer 36 of Fig. 4, stretch on the first polycrystalline silicon layer 6 in the vertical direction in Fig. 7.

15 A power-supply line V_{CC-L} runs in the lateral direction of Fig. 7 to supply power-supply voltage V_{CC} through the contact hole CH_0 to the polycrystalline silicon layer 6 which serves as one electrode of the memory capacitor C_s .

20 On the other hand, data lines DL_{1-1} , $\overline{DL}_{1-1}$ composed of the aluminum layer 10 of Fig. 4 run nearly in parallel with the power-supply line V_{CC-L} as shown in Fig. 7. The data line DL_{1-1} is connected to the drain region of MISFET Q_M in the memory cell M-CEL via a contact hole CH_1 , and the data line $\overline{DL}_{1-1}$ is connected to the drain region
25 of MISFET Q_M in another memory cell M-CEL via a contact

hole CH_2 . Further, the data lines DL_{1-2} , $\overline{DL}_{1-2}$ run in the lateral direction in Fig. 7 like the data lines DL_{1-1} and $\overline{DL}_{1-1}$, and are connected to the drain regions of the MISFETs Q_M in the memory cells M-CEL at predetermined portions through contact holes.

Next, the dummy cells D-CEL shown in Fig. 7 are constructed as mentioned below.

The field insulating film 2 is formed on a portion of the surface of the semiconductor substrate 1, and the gate insulating film 3 is formed on another portion on the surface of the semiconductor substrate 1.

The first polycrystalline silicon layers 15a, 15b run on the field insulating film 2 and the gate insulating film 3 in the vertical direction of Fig. 7 being separated away from each other. The widths of the first polycrystalline silicon layers 15a, 15b are very important from the standpoint of determining the capacity of capacitor Cds in the dummy cell D-CEL. The n^+ -type semiconductor region 14 is positioned between the first polycrystalline silicon layer 15a and the first polycrystalline silicon layer 15b. The n^+ -type semiconductor region 14 is used as a common earth line for a plurality of dummy cells D-CEL.

Further, a dummy word line DWL_{1-1} composed of a multi-layer wiring of the secondary polycrystalline silicon layer 17, the molybdenum silicide layer 30 and the molybdenum

layer 37 of Fig. 5, runs on the first polycrystalline silicon layer 15a. The dummy word line DWL_{1-1} constitutes a gate electrode of MISFET Q_{D1} in the dummy cell D-CEL.

— On the other hand, a control signal line ϕ_{dc-L_1} of a multi-layer wiring composed of the second polycrystalline silicon layer 18, the molybdenum silicide layer 31 and the molybdenum layer 38 of Fig. 5, runs in parallel with the dummy word line DWL_{1-1} being separated away therefrom, so that the discharge control signal ϕ_{dc} shown in Fig. 5A can be applied. The control signal line ϕ_{dc-L_2} forms a gate electrode of MISFET Q_{D2} in the dummy cell D-CEL.

Similarly, a dummy word line DWL_{1-2} and a control signal line ϕ_{dc-L_2} run in parallel with the dummy word line DWL_{1-1} and the control signal line ϕ_{dc-L_1} .

Further, the data lines DL_{1-1} , $\overline{DL}_{1-1}$, DL_{1-2} , $\overline{DL}_{1-2}$ composed of aluminum layer stretch from the memory array M-ARY as shown in Fig. 7. The data line $\overline{DL}_{1-1}$ is connected to the drain region of MISFET Q_{D1} in the dummy cell D-CEL via a contact hole CH_3 , and the data line $\overline{DL}_{1-2}$ is also connected to the drain region of MISFET Q_{D1} of another dummy cell D-CEL through a contact hole CH_4 .

[Lay-out pattern of peripheral circuits]

Fig. 10 shows a lay-out pattern of a portion of the peripheral circuits, for example, a portion of the sense amplifier SA_1 of Fig. 2.

In Fig. 10, AR denotes an active restore portion, and PC denotes a circuit for precharging the data lines.

Two active restores AR_1 shown in Fig. 2 are provided in the active restore portion AR. Namely, one active restore is formed on the side of arrow A in Fig. 10, and another active restore is formed on the side of arrow B. An active restore control signal line ϕ_{rg} -L consisting of a polycrystalline silicon layer, a molybdenum silicide layer and a pure molybdenum layer, a line ϕ_{rg} -L consisting of an aluminum layer, and a power-supply line V_{CC} -L consisting of an aluminum layer, are arrayed in common for the active restores in the active restore portion AR as shown in Fig. 10.

On the other hand, the precharging circuit PC contains a circuit for precharging the two data lines that correspond to the two active restores. In the precharging circuit PC are arrayed a potential line V_{DP} -L composed of an aluminum layer, a precharge control signal line ϕ_{PC} -L, and data lines DL_{1-1} , $\overline{DL}_{1-1}$, DL_{1-2} , $\overline{DL}_{1-2}$ composed of an aluminum layer which run on the memory array M-ARY of Fig. 2, as shown in Fig. 10.

MISFETs Q_{S1} to Q_{S7} and capacitors C_{B11} , C_{B12} of Fig. 2 are arrayed as shown in Fig. 10.

Next, a process for producing an n-channel D-RAM will be described below with reference to Figs. 11A to 11S.

In each of the drawings, X_1 stands for a section view of the memory array M-ARY of Fig. 7 along X_1-X_1 , X_2 stands for a section view of the active restore AR of Fig. 10 along X_2-X_2 , and X_3 stands for a section view of the active restore AR of Fig. 10 along X_3-X_3 .

(Step for forming an oxide film and an oxidation-resistant film)

As shown in Fig. 11A, an oxide film 102 and an insulating film, i.e., an oxidation-resistant film 103 which does not permit the passage of oxygen, are formed on the surface of a semiconductor substrate 101.

A p-type single crystalline silicon (Si) substrate having a crystalline plane (100), a silicon dioxide (SiO_2) film and a silicon nitride (Si_3N_4) film are preferably used for forming the semiconductor substrate 101, the oxide film 102 and the oxidation-resistant film 103.

The SiO_2 film 102 is formed by the surface oxidation of the silicon substrate 101 to a thickness of about 500 angstroms, because of the reasons mentioned below. That is, when the Si_3N_4 film 103 is formed directly on the surface of the silicon substrate 101, the surface of the silicon substrate 101 tends to be thermally distorted due to the difference in the thermal expansion coefficient between the silicon substrate 101 and the Si_3N_4 film 103. Conse-

quently, crystalline defect is given to the surface of the silicon substrate 101. In order to prevent this defect, the SiO_2 film 102 is formed on the surface of the silicon substrate 101 prior to forming the Si_3N_4 film 103.

On the other hand, the Si_3N_4 film 103 which will be used as a mask for selective oxidation of the silicon substrate 101, is formed to a thickness of about 1400 angstroms by the CVD (chemical vapor deposition) method, as will be mentioned later in detail.

(Step for selectively removing oxidation-resistant film and for injecting ions)

A photoresist film 104 which serves as an etching mask is selectively formed on the surface of the Si_3N_4 film 103 that is to be selectively removed from the surface of the silicon substrate 101 on which will be formed a relatively thick insulating film, i.e., a field insulating film. Under this condition, the exposed portions of the Si_3N_4 film 103 are removed by the plasma etching method which features good etching precision.

Then, impurities of the same type of conductivity as the substrate 101, i.e., p-type impurities are introduced into the silicon substrate 101 through the SiO_2 film 102 that is exposed at portions which are not covered with the photoresist film 104 as shown in Fig. 11B, so that

a so-called inverted layer of the type of conductivity opposite to that of the substrate will not be formed on the surface of the substrate 101 on which the field insulating film is formed. The p-type impurities can be introduced preferably by the ion-injection method. For example, boron ions which are p-type impurities can be injected into the silicon substrate 101 at an injection energy of 75 KeV. In this case, the dosage of ions will be 3×10^{12} atoms/cm².

10 (Step for forming field insulating film)

A field insulating film 105 is selectively formed on the surface of the silicon substrate 101. Namely, after the photoresist film 104 is removed, the surface of the silicon substrate 101 is selectively oxidized by thermal oxidation using the Si₃N₄ film 103 as a mask, to form the SiO₂ film 105 (hereinafter referred to as a field SiO₂ film) of a thickness of about 9500 angstroms, as shown in Fig. 11C. When the field SiO₂ film 105 is being formed, the injected boron ions diffuse into the silicon substrate 101, thereby to form a p-type inversion preventing layer (not shown) of a predetermined depth beneath the field SiO₂ film 105.

(Step for removing oxidation-resistant film and oxide film)

The Si₃N₄ film 103 is removed using, for example, a hot phosphoric acid (H₃PO₄) solution in order to expose

the surface of the silicon substrate 101 of the portions where the field SiO_2 film 105 is not formed. Then, the SiO_2 film 102 is removed by using a hydrofluoric acid (HF) solution, so that the surface of the silicon substrate 101 is selectively exposed as shown in Fig. 11D.

(Step for forming a first gate insulating film)

A first gate insulating film 106 is formed on the exposed surfaces of the silicon substrate 101 as shown in Fig. 11E in order to form a dielectric layer for the capacitors C_s , D_{ds} in the memory cells M-CEL and in the dummy cells D-CEL. Namely, the surface of the exposed silicon substrate 101 is thermally oxidized to form the first gate insulating film 106 having a thickness of about 430 angstroms on the surface of the silicon substrate 101. Therefore, the first gate insulating film 106 consists of SiO_2 .

(Step for adhering a first conductor layer)

A first conductor layer 107 is formed on the whole surface of the silicon substrate 101 as shown in Fig. 11F so that it can be used as one electrode of capacitors in the memory cells and in the dummy cells. Namely, a polycrystalline silicon layer 107 which serves as the first conductor layer is formed on the whole surface of the silicon substrate 101 by the CVD method. The polycrystalline silicon layer 107 has a thickness of about 4000 angstroms.

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Then, in order to reduce the resistance of the polycrystalline silicon layer 107, n-type impurities, such as phosphorus ions, are introduced into the polycrystalline silicon layer 107 by the diffusion method. Therefore, the polycrystalline silicon layer 107 possesses a resistivity of about 16 ohms/cm².

(Step for selectively removing the first conductor layer)

In order to form the first conductor layer, i.e., the first polycrystalline silicon layer 107 into electrodes of a predetermined shape, the first polycrystalline silicon layer 107 is selectively removed by the photoetching method as shown in Fig. 11G, thereby to form electrodes 108.

The first polycrystalline silicon layer 107 can be selectively removed by plasma etching which features good etching precision. Therefore, the exposed first SiO₂ gate film 106 is subjected to etching, so that surfaces of the silicon substrate 101 are partially exposed.

(Step for forming a second gate insulating film)

A second gate insulating film 109 is formed on the exposed surface of the silicon substrate 101 as shown in Fig. 11H in order to obtain a gate insulating film for the MISFET's in the memory cells M-CEL, dummy cells D-CEL, and in the peripheral circuits. Namely, the exposed surface of the silicon substrate 101 is thermally oxidized to form a second gate insulating film 109 of a thickness of about

530 angstroms on the surface of the silicon substrate 101.

Therefore, the second gate insulating film 109 consists of SiO_2 . The surface of the electrodes 108 composed of the

first polycrystalline silicon is also oxidized simultaneously with the formation of the second gate insulating

film, i.e., simultaneously with the formation of the second SiO_2 gate film 109; an SiO_2 film 110 having a thickness of

about 2200 angstroms is formed on the surface of the electrodes 108. The SiO_2 film 110 serves as an insulating

layer between the electrodes 108 and the electrodes composed of a second polycrystalline silicon that will be mentioned later.

(Step for injecting ions for controlling low threshold voltage)

P-type impurities are introduced into the surface of the substrate through the second SiO_2 gate film 109 by the ion-injection method as shown in Fig. 11I in order to

define a threshold voltage of MISFETs Q_{S1} to Q_{S3} , Q_{S6} and Q_{S7} which are shown in Fig. 2 and which have a low

threshold voltage. Boron ions will be used as the p-type impurities. The energy for injection will be 75 KeV, and the dosage of ions will preferably be 2.4×10^{11} atoms/cm².

In this case, ions are injected without using a selection mask. Therefore, boron ions are also introduced into the surfaces of the substrate where other MISFET's are to

be formed, such as Q_M , Q_{D1} , Q_{D2} , Q_{D4} , Q_{D5} .

(Step for injecting ions for controlling high threshold voltage)

5 A mask for ion injection, i.e., a photoresist film 111 is formed on the second SiO_2 gate film 109 on the channel regions of MISFET Q_{S1} to Q_{S3} , Q_{S6} and Q_{S7} as shown in Fig. 11J, and boron ions are injected under this condition in order to define a threshold voltage of MISFET's having a threshold voltage greater than that of MISFETs Q_{S1} to Q_{S3} ,
10 Q_{S6} and Q_{S7} shown in Fig. 2, i.e., in order to define a threshold voltage of MISFET Q_M in the memory cells, MISFETs Q_{D1} , Q_{D2} in the dummy cells, and MISFETs Q_{S4} , Q_{S5} in the active restores. The injection energy will be 75 KeV, and a preferred dosage of ions will be 1.0×10^{11}
15 atoms/cm².

Consequently, the impurity concentration is further increased in the surface of the portions of the substrate where MISFETs Q_M , Q_{D1} , Q_{D2} , Q_{S1} and Q_{S5} are to be formed. Therefore, these MISFET's have a high threshold value.

20 (Step for forming holes for direct contact)

Holes for directly connecting one electrode 25 of the capacitor C_{B11} to the n^+ -type semiconductor region 22 of MISFET Q_{S4} as mentioned with reference to Fig. 6 are formed, i.e., so-called direct contract holes CH_{100} , are formed by
25 selectively etching the second SiO_2 gate film using the

photoresist film 112 as a mask, as shown in Fig. 11K.

(Step for adhering a second conductive layer)

A second conductive layer is formed on the whole surface of the silicon substrate 101 so that it can be used as a gate electrode and a wiring layer for all of the MISFET's. Namely, a polycrystalline silicon layer, a silicide layer of silicon and a refractory metal, and a pure refractory metal layer are formed as a second conductive layer, as shown in Fig. 11L. First, a polycrystalline silicon layer 113 is formed on the whole surface of the silicon substrate 101 by the CVD method (chemical vapor deposition method). The polycrystalline silicon layer 113 has a thickness of about 1500 to 2500 angstroms. Then, n-type impurities such as phosphorus ions are introduced into the polycrystalline silicon layer 113 by the diffusion method, in order to decrease the resistance. Some of the phosphorus ions are introduced into the silicon substrate 101 through direct contact holes CH₁₀₀. Therefore, there is no need of forming high-concentration regions for ohmic contact.

Then, a silicide layer 128 of silicon and a refractory metal is formed on the whole surface of the polycrystalline silicon layer 113. Molybdenum will be used as the refractory metal. Molybdenum and silicon are deposited on the polycrystalline silicon layer by the co-sputtering method

in order to form a mixed layer of silicon and molybdenum. The silicon content will be, for example, 10 % by weight.

The sputtering conditions will consist of a vacuum degree of smaller than 40 μ Pa before argon gas is

5 introduced, an argon-gas pressure of 4.0 Pa when the sputtering is being effected, a molybdenum deposition rate of 0.1 to 0.8 nm/sec., and a silicon deposition rate of 0.1 nm/sec or less. The molybdenum silicide layer 128 consisting of silicon and molybdenum has a thickness of
10 about 1000 angstroms.

A pure refractory metal layer 130 is then formed on the whole surface of the molybdenum silicide layer 128.

Molybdenum will be used as the refractory metal. The sputtering method is used for forming the refractory metal
15 layer. In this case, the sputtering is effected under the same conditions as above. The molybdenum layer has a thickness of about 1500 angstroms.

(Step for selectively removing the second conductive layer)

The second conductive layer, i.e., the second polycrystalline silicon layer 113, molybdenum silicide layer
20 128 and the molybdenum layer 130 are selectively removed to form predetermined electrodes or wirings by the dry-etching method using a photoresist. A gas consisting, for example, of $\text{CF}_4 + \text{O}_2$ is used as an etching gas. The
25 above-mentioned three layers are removed by etching

(plasma etching) or by plasma discharge in the presence of the gas. First, the molybdenum layer is subjected to the etching, the molybdenum silicide layer is subjected to the etching next, and the polycrystalline silicon layer is subjected to the etching maintaining the same shape in the presence of the same gas. Then, the annealing is effected in an nitrogen atmosphere. Owing to the annealing, molybdenum and silicon are uniformly dispersed in the molybdenum silicide layer 129. The polycrystalline silicon layer 114, the molybdenum silicide layer 129, and the molybdenum layer 131, that are formed in the shapes as shown in Fig. 11M by the plasma etching, form word lines WL_{1-1} to WL_{1-6} , dummy word lines DWL_{1-1} , DWL_{1-2} , and control signal lines ϕ_{dc-L_1} , ϕ_{dc-L_2} , which are shown in Fig. 7, and further form active restore control signal line ϕ_{rg-L} , electrode 114 for the capacitors C_{B11} , C_{B12} , and gate electrodes for the MISFETQ_{S1} and Q_{S2}, which are shown in Fig. 10. In Fig. 11M, furthermore, the exposed second SiO₂ gate film 109 is removed, to expose the surface of the silicon substrate 101.

(Step for oxidizing the surface)

An SiO₂ film 115 of a thickness of about 100 angstroms is formed by the chemical vapor deposition (CVD) method on the surface of the exposed silicon substrate 101, as shown

in Fig. 11N, so that the surfaces where source regions and drain regions of MISFET's are to be formed, will not be contaminated. Simultaneously with the formation of the SiO_2 film 115, an SiO_2 film 116 having a thickness of about 100 angstroms is also formed by the CVD method, as shown in Fig. 11N, on the surfaces of word lines WL_{1-1} to WL_{1-6} , dummy word lines DWL_{1-1} , DWL_{1-2} , control signal lines $\phi_{\text{dc}}\text{-L}_1$, $\phi_{\text{dc}}\text{-L}_2$, electrode 114 of the capacitors C_{B11} , C_{B12} , and gate electrodes of MISFETs Q_{S1} to Q_{S3} , which consist of the second polycrystalline silicon layer 113, molybdenum silicide layer 128 and molybdenum layer 130.

In forming the SiO_2 films 115 and 116, the following measure is taken in order to prevent the molybdenum layer 114 from being oxidized and sublimated.

First, the semiconductor substrate 101 is set into a device for forming the SiO_2 film by the CVD method. In this case, the temperature in the device is lower than 200°C . Then, nitrogen gas is allowed to flow sufficiently so that no oxygen is present in the device. Then, the SiO_2 film is formed by elevating the temperature in the device to about 400° to 450°C . Concretely speaking, $\text{SiH}_4 + \text{O}_2$ is allowed to flow with the nitrogen gas as a carrier gas; the $\text{SiH}_4 + \text{O}_2$ gas is thermally decomposed and is reacted. Oxygen introduced at this moment does not react with molybdenum but reacts with silicon to form an SiO_2 film

on the surface of the substrate.

(Step for forming source and drain regions)

5 N-type impurities such as arsenic ions are introduced into the silicon substrate 101 through the SiO_2 film 115, as shown in Fig. 110, in order to selectively form source and drain regions of MISFET's in the silicon substrate 101. The n-type impurities can be introduced preferably by the ion-injection method. For example, arsenic ions are injected into the silicon substrate 101 at an injection energy of 80
10 KeV. In this case, the dosage of ions will be 1×10^{16} atoms/cm².

(Step for forming contact holes)

Contact holes are formed in the SiO_2 film to connect the source and drain regions to the third conductive layer.
15 Namely, contact holes CH_{101} to CH_{104} are formed as shown in Fig. 11P by selectively etching the SiO_2 film 115 using a predetermined mask. Here, the contact hole CH_{102} corresponds to the contact hole CH_1 of Fig. 7.

(Step for forming interlayer insulating film)

20 An interlayer insulating film is formed on the whole surface of the silicon substrate 101. That is, an interlayer insulating film 118, for example, a phosphorus silicate glass (PSG) film having a thickness of about 8000 angstroms is formed on the whole surface of the silicon substrate 101,
25 as shown in Fig. 11Q. The PSG film 118 also serves as a

sodium ion getter which affects the characteristics of MISFET's.

(Step for forming contact holes)

5 Contact holes are formed in the PSG film 118 in order to connect the second polycrystalline silicon layer to the third conductive layer, and the source and drain regions to the third conductive layer. That is, the PSG film 118 is subjected to the selective etching to form contact holes CH_{101} to CH_{104} , as shown in Fig. 11R. The mask used for forming the contact holes CH_{101} to CH_{104} is the same as the mask used for forming the contact holes CH_{101} to CH_{104} in the aforementioned step for forming contact holes.

Therefore, the PSG film 118 is thermally treated at a temperature of about $1000^{\circ}C$ in order to flatten it. Arsenic ions injected through the heat treatment are diffused to form n^{+} -type semiconductor regions 119 to 126 having a predetermined depth. The n^{+} -type semiconductor regions 119 to 126 serve as source and drain regions.

Here, the contact holes formed in the SiO_2 film 115 in the aforementioned step, may be formed simultaneously with the formation of contact holes in the PSG film 118. However, the PSG film 118 is subjected to the etching before the contact holes are completely formed in the SiO_2 film 115. In other words, the PSG film 118 is subjected to over-etching. In order to prevent the

over-etching, therefore, the contact holes should be formed in the PSG film 118 through a step different from the step for forming the contact holes in the SiO_2 film 115.

5 (Step for forming a third conductive layer)

A third conductive layer, for example, an aluminum layer having a thickness of about 12000 angstroms is formed on the whole surface of the silicon substrate 101, in order to form the power-supply line V_{CC-L} , and data lines DL_{1-1} , $\overline{DL}_{1-1}$, DL_{1-2} , and $\overline{DL}_{1-2}$, that are shown in Fig. 7. The aluminum layer is then subjected to the selective etching to form a power-supply line V_{CC-L} , data line DL_{1-1} and wiring layer 127, as shown in Fig. 11S.

15 According to the above-mentioned embodiment of the present invention, it is possible to realize a D-RAM IC, i.e., a semiconductor integrated circuit device having a wiring layer of a small resistivity and fast signal transmission speed. Further, the effects (1) to (3) obtained in the first embodiment can also be equally
20 obtained by this embodiment. According to this embodiment, in particular, the first conductive layer consists of polycrystalline silicon. However, since the first conductive layer is always impressed with a predetermined voltage or is grounded, there arises no problem even when it has
25 a high resistivity. Rather, the first conductive layer

composed of polycrystalline silicon makes it possible to form a dense insulating film (SiO_2 film) by thermally oxidizing the surface thereof.

According to the embodiment of the present invention, furthermore, a semiconductor integrated circuit device having the above-mentioned effects can be obtained without passing through complicated manufacturing steps. Namely, according to the embodiment of the present invention, the wiring layer consisting of polycrystalline silicon layer 114, molybdenum silicide layer 129 formed on the layer 114, and molybdenum layer 131 formed on the layer 129, serves as an electrode that comes into direct contact with the n^+ -type semiconductor region 22, serves as a gate electrode for MISFET's, and serves as one electrode of MIS capacitors. When the individual electrodes are to be formed using separate materials, i.e., when the electrode that comes into direct contact with the semiconductor region, gate electrode of MISFET's, and one electrode of MIS capacitors, are to be formed using separate materials, increased number of manufacturing steps will be necessary.

Further, simultaneous formation of one electrode of MIS capacitors and the electrode that comes into contact with the semiconductor region 22, helps increase the degree of integration. That is, if these electrodes are made of

different materials, a contact area must be provided between the two electrodes. Therefore, the above-mentioned manufacturing steps are effective to increase the density of wiring. The molybdenum silicide layer which serves as one electrode of MIS capacitors presents no problem.

The present invention should in no way be limited to the above-mentioned embodiments only. For example, in addition to using molybdenum silicide (MoSi), it is also allowable to use titanium silicide (TiSi_2), tantalum silicide (TaSi) or tungsten silicide (WSi) as a second conductive layer for forming multi-layer wiring.

In addition to molybdenum, furthermore, it is also allowable to use titanium, tantalum or tungsten as a refractory metal.

Furthermore, the steps of Figs. 111 to 110 in the above-mentioned embodiment can be rearranged as mentioned below. First, the polycrystalline silicon layer 113, the silicide layer 128 of silicon and refractory metal, and the pure refractory metal layer 131 are laminated in the order mentioned on the SiO_2 gate film 109 and on the SiO_2 field film 105, as shown in Fig. 111. Then, the above-mentioned three layers are selectively removed by dry etching to form a wiring layer or gate electrode. Source and drain regions are then formed beneath the SiO_2 gate film 109 using the wiring layer as a mask. These

regions are formed by the ion implantation method.

According to the present embodiments, therefore, it is possible to obtain semiconductor integrated circuit devices having a high density which results from the self-matching property, and having a wiring layer with small resistivity and short signal transmission time.

Attention is drawn to Application No. 83.31916 (Serial No. 2,134,706) which has been divided out of the present Application in which there is claimed

10 a method of fabricating a semiconductor memory device including a memory cell array having a plurality of memory cells formed on a semiconductor substrate wherein each of said memory cells has a capacitor and an MIS-type field effect transistor and wherein each of said memory cells is
15 coupled to at least one of a plurality of data lines, and a peripheral circuit formed on said semiconductor substrate wherein said peripheral circuit is associated with said memory cell array and wherein said peripheral circuit is constructed of a plurality of MIS-type field effect
20 transistors and interconnecting lines at least one of which is contacted with one semiconductor region of one of said MIS-type field effect transistors, comprising the steps of:

forming a first layer of polycrystalline silicon over
25 substantially the entire area of one main surface of a semiconductor substrate, said first layer having portions overlying first insulating films formed on selected first areas of said main surface in which said capacitors are



to be formed;

patterning said first layer to form one electrode of each of said capacitors in each first area;

forming a second layer of polycrystalline silicon over
5 substantially the entire area of said main surface, said second layer extending over an insulating film formed on said patterned first layer of polycrystalline silicon and extending on gate insulating films formed on selected second areas of said main surface in which said MIS-type
10 field effect transistors for said memory cells and peripheral circuit are to be formed, said second layer having a portion which is contacted with a portion of one of said second areas;

forming over said second layer a third layer which is
15 composed of a refractory metal; and

patterning said successive second and third layers to form gate electrodes of said MIS-type field effect transistors and said word lines and to form said inter-connecting lines at least one of which is contacted with
20 the portion of said second area serving as said semiconductor region of said MIS-type field effect transistor.



CLAIMS:

1. A semiconductor memory integrated circuit device comprising data lines extending in parallel with each other, word lines extending in a direction generally at right angles to said data lines, and memory cells coupled
5 between said data lines and said word lines, wherein each of said word lines comprises three successive layers of a polycrystalline silicon layer, a refractory metal silicide layer formed on said polycrystalline silicon layer, and a refractory metal layer formed on said refractory metal
10 silicide layer.
2. A semiconductor integrated circuit device comprising a semiconductor substrate having one main surface, an insulating film formed on said main surface of said semiconductor substrate, said insulation film having a hole
15 exposing a portion of said main surface, a semiconductor region of one conductivity type formed at an area including said exposed portion in said semiconductor substrate, and a conductive layer in contact with said semiconductor region at said exposed portion and extending over said
20 insulating film, wherein said conductive layer comprises three successive layers of a polycrystalline silicon layer in contact with said semiconductor region at said exposed region and extending on said insulating film, a refractory metal silicide layer, and a refractory metal layer, said
25 polycrystalline silicon layer being doped with impurities

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of the same conductivity as that of said semiconductor region.

3. A semiconductor integrated circuit device comprising an insulating film formed on one main surface of a semiconductor substrate, said insulating film including a thick field insulating film and a thin gate insulating film, a gate electrode strip selectively formed on said gate insulating film and extending on said field insulating film, source and drain regions formed in said semiconductor substrate on both sides of said gate electrode strip, and a wiring strip contacting at least one of the source and drain regions and extending on said field insulating film, wherein the gate electrode strip and the wiring strip each comprise three successive layers of a polycrystalline silicon layer, a refractory metal silicide layer formed on said polycrystalline silicon layer, and a refractory metal layer formed on said refractory metal silicide layer.

4. A semiconductor integrated circuit device according to claim 2 or 3, wherein said refractory metal layer is a molybdenum layer.

5. A semiconductor integrated circuit device according to any one of the proceeding claims 2 to 4, wherein the refractory metal silicide layer consists of one of the following:

(a) silicon and molybdenum,



- (b) silicon and tungsten,
- (c) silicon and tantalum.

6. A MIS-type field effect transistor comprising a gate insulating film formed on one main surface of a semiconductor substrate, a gate electrode selectively formed on said gate insulating film, said gate electrode having two sides, source and drain respectively regions formed in the semiconductor substrate on the two sides of said gate electrode, and a contacting electrode which is contacted with at least one of said source and drain regions, wherein said gate electrode comprises three successive layers of a polycrystalline silicon layer formed on said gate insulating film, a refractory metal silicide layer formed on said polycrystalline silicon layer, and a refractory metal layer formed on said refractory metal silicide layer, and wherein said source and drain regions are aligned with respective opposite edge portions of said gate electrode, and said contacting electrode comprises three successive layers of a polycrystalline silicon layer contacted with at least one of said source and drain regions, a refractory metal silicide layer for the contact electrode which is formed on said polycrystalline silicon layer and in contact with at least one of said source and drain regions, and a refractory metal layer on said refractory metal silicide layer for the contact electrode.

7. A MIS-type field effect transistor according to claim 6, wherein each of said three successive layers has



substantially the same thickness.

8. A process for producing semiconductor devices including the following steps:

(a) forming an insulating film on one main surface
5 of a semiconductor substrate;

(b) forming a polycrystalline silicon layer on said insulating film;

(c) forming a deposited layer of silicon and a refractory metal by simultaneously sputtering silicon and
10 a refractory metal on said polycrystalline silicon layer;

(d) forming a refractory metal layer on the deposited layer of silicon and the refractory metal; and

(e) annealing said polycrystalline silicon layer, said deposited layer and said refractory metal layer.

15 9. A process for producing semiconductor devices according to claim 8, wherein said polycrystalline silicon layer, said deposited layer and said refractory metal layer are subjected to selective etching after they have been formed.

20 10. A process for producing semiconductor devices by forming an insulating film on one main surface of a semiconductor substrate, and by selectively forming a gate electrode on the insulating film, wherein said gate electrode is formed by the following procedure: a
25 polycrystalline silicon layer is formed by the CVD method on said insulating film, silicon and a refractory metal



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are deposited on said polycrystalline silicon layer by the co-sputtering method, a refractory metal layer is formed on the deposited layer by sputtering, and the polycrystalline silicon layer, the deposited layer and the refractory metal layer are selectively removed and annealed.

11. A process for producing semiconductor devices according to claim 10, wherein after said gate electrode is formed, a source region and a drain region are formed in the semiconductor substrate one on each side of said gate electrode.

12. A process for producing semiconductor devices according to claim 11, wherein said source and drain regions are formed by the ion implantation method.

13. A process for producing semiconductor devices substantially as any described herein with reference to the accompanying drawings.

14. A semiconductor integrated circuit device substantially as any described herein with reference to and as illustrated in the accompanying drawings.

15. A semiconductor integrated circuit device produced by a process according to any one of claims 8 to 13.
