

ABSTRACT

A semiconductor device can include a front-end-of-line region on a substrate, where the front-end-of-line region can include an electrostatic discharge protection circuit and an integrated circuit electrically connected to the electrostatic discharge protection circuit. A back-end-of-line region can be on the front-end-of-line region and an electrostatic discharge protection pattern can be on a scribe region of the substrate. The electrostatic discharge protection pattern can include a lower pattern extending horizontally and a side cross-sectional surface defined by a height and a width of the lower pattern, where the side cross-sectional surface can be exposed outside the back-end-of-line region. A via can be electrically connected to the lower pattern and extend perpendicularly to the substrate and an upper pattern can be electrically connected to the via.

FIG. 4A