

METHODS FOR ENHANCING THE FORMATION OF NICKEL MONO-SILICIDE BY REDUCING THE FORMATION OF NICKEL DI-SILICIDE

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/576,559, filed on June 2, 2004, the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuit and semiconductor device fabrication and, more particularly, to methods for reducing stress in silicon to enhance the formation of nickel mono-silicide films formed thereon.

BACKGROUND OF THE INVENTION

[0003] Self-aligned silicide (salicide) technology is required in modern integrated circuit and semiconductor device fabrication to lower the resistance of polysilicon gates, sources and drains to reduce RC delay, i.e., the gate speed performance index wherein less delay produces increased gate speed performance. An example of a well known silicide technology is cobalt silicide (CoSi_2). CoSi_2 technology is commonly used for sub quarter micron and beyond technology. However, the agglomeration effect of CoSi_2 on very narrow line polysilicon gates that are less than ~ 42 nanometers, often limits its extendibility to the fabrication of shorter gates.

[0004] Nickel mono-silicide (NiSi) technology appears to be emerging as a dominant solution to very narrow line polysilicon gates because it provides superior sheet

resistance (R_s) for narrow line polysilicon gates, less junction leakage, less silicon (Si) consumption, and can even improve the drive current (I_{dsat}) of an NFET or PFET.

[0005] There are, however, some concerns about NiSi because it may not form completely or at all when the single crystal Si or Si containing substrate is under tensile stress and instead, undesirable nickel di-silicide ($NiSi_2$) forms. $NiSi_2$ is undesirable because it increases the resistance of the silicide. Moreover, faceted $NiSi_2$ may form deeply in the Si substrate thereby producing junction leakage. In addition, $NiSi_2$ can easily form over a wide temperature range. For example, Ni will form epitaxial $NiSi_2$ on a p-type Si crystal substrate as low as 225 °C, which decreases the process window.

[0006] The tensile stress in the single crystal Si or Si containing substrate may be due to the p-type dopant atoms in the substrate. For example, boron is commonly used as a p-type dopant atom in Si. Boron has a smaller atomic radius than Si, which causes strain in the Si crystal lattice. Tensile stress in Si may also be due to geometry and thermal effects.

[0007] Accordingly, methods are needed which allow NiSi to be implemented successfully in modern integrated circuit and semiconductor device fabrication.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A-1C are sectional views illustrating a first method of fabricating a PMOS semiconductor device according to the present invention.

[0009] FIG. 2A is a graph showing active carrier concentration versus implantation depth without a strain compensation implant.

[0010] FIG. 2B is a graph showing strain versus depth of implantation without strain compensation.

[0011] FIG. 3A is a graph showing active carrier concentration versus implantation depth after performing the strain compensation implant of the present invention.

[0012] FIG. 3B is a graph showing strain versus depth of implantation strain compensation.

[0013] FIGS. 4A-4C are sectional views illustrating an alternate method of fabricating a PMOS semiconductor device according to the present invention.

[0014] FIGS. 5A-5C are sectional views illustrating another method of fabricating a PMOS semiconductor device according to the present invention.

[0015] FIGS. 6A-6C are sectional views illustrating still another method of fabricating a PMOS semiconductor device according to the present invention.

[0016] FIGS. 7A-7C are sectional views illustrating yet another method of fabricating a PMOS semiconductor device according to the present invention.

[0017] FIGS. 8A-8C are sectional views illustrating yet another method of fabricating a PMOS semiconductor device according to the present invention.

[0018] FIGS. 9A-9C are sectional views illustrating yet another method of fabricating a PMOS semiconductor device according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] FIGS. 1A-1C are sectional views illustrating a method of fabricating an N- or P-MOS semiconductor device according to the present invention. As illustrated in FIG. 1A, the method commences with the formation of a gate structure 130 over a p-or n-type single crystal Si substrate 120 or any other substrate containing Si such as SiGe, followed by the formation of first and second non-conductive spacers 160a, 160b along opposing

side walls of the gate structure 130. The gate structure 130 (and the other gate structures referred to further on) may include a gate oxide 132, such as silicon dioxide (SiO_2), disposed over the substrate 120 and a gate conductor 134, such as polysilicon, disposed over the gate oxide 132. The gate structure 130 may be formed using conventional methods well known in the art. The spacers 160a, 160b may be composed, for example, of a conventionally fabricated oxide or nitride layer.

[0020] A source/drain implantation process is performed to form self-aligned first and second p⁺ source/ drain regions 170a and 170b in the substrate 120. The source/drain ion implantation process may be performed conventionally using a p-type dopant such as B and BF_2 . LDD (lightly doped drain) areas in the case of a PMOS device (shown) or a halo implant area in the case of an NMOS device, are formed as part of source/drain extensions 171a and 171b with a p-type dopant, before the spacer or after the source/drain process. Note that the “source/drain region” is used herein to refer to a source/drain region and/or a source/drain extension region.

[0021] The B or BF_2 implant at the source/drain regions of the substrate increases the tensile stress of the Si or substrate containing Si, because a B atom has an atomic radius that is much smaller than the atomic radius of an Si atom. The tensile stress or strain may be compensated for, according to the present invention, by implanting additional atoms at the source/drain regions which have atomic radii that are greater than the atomic radius of the Si atom and which are capable of maintaining the p⁺ conductivity. Such atoms may be the atoms of one or more Group IV elements, Group II elements, and Group III elements, and combinations thereof. The strain compensation implantation process may

be performed either before or after the source/drain implantation process. FIG. 1B depicts the device after the source/drain and strain compensation implantations.

[0022] In order to maintain proper device function, the active carrier concentration and profile should be the substantially same after performing the strain compensation implant of the present invention as shown graphically in FIGS. 2A and FIG. 3A. Specifically, FIG. 2A shows the active carrier concentration versus implantation depth without a strain compensation implant, and FIG. 3A shows substantially the same active carrier concentration versus implantation depth after performing the strain compensation implant of the present invention. As can be seen in FIGS. 2B and 3B, which graphically show strain versus depth of implantation without strain compensation (FIG. 2B) and with strain compensation (FIG. 3B), the strain compensation implant of the present invention significantly reduces the strain in the source/drain regions of the substrate. One of ordinary skill in the art will appreciate that the strain in the source/drain regions of the substrate does not have to be completely compensated to achieve nickel mono-silicide enhancement.

[0023] The active carrier concentration and profile may be maintained with the strain compensation implant of the present invention by adjusting the B or BF₂ source/drain implant dosage and the group II/III/ IV element(s) strain compensation implant dosage according to the size of their atomic radii. For example, if the B or BF₂ source/drain implant dosage is about $3 \times 10^{15}/\text{cm}^2$ without strain compensation, then the total active carrier source/drain dosage with the strain compensation implant may be calculated as follows in the below examples:

For B and group IV Ge:

Atomic radii of the atoms are: $R_{\text{Ge}} = 1.22 \text{ \AA}$, $R_{\text{Si}} = 1.11 \text{ \AA}$, $R_{\text{B}} = 0.8 \text{ \AA}$

$R_{Si} = C * R_B + (1-C) * R_{Ge}$
 $C = 0.26$ where C is a preselected concentration ratio that allows the correct ratio of source/drain dopant to strain relief dopant

$$\text{Dose (Ge)} : \text{Dose (B)} = (0.74)^3 : (0.26)^3 \cong 23 : 1$$

$$\text{Total active carrier source/drain dosage} = \text{Dose (Ge)} + \text{Dose (B)}$$

For B and group III In:

Atomic radii of the atoms are: $R_{In} = 1.44 \text{ \AA}$, $R_{Si} = 1.11 \text{ \AA}$, $R_B = 0.8 \text{ \AA}$

$$R_{Si} = C * R_B + (1-C) * R_{In}$$

$$C = 0.516$$

$$\text{Dose (In)} : \text{Dose (B)} = (0.484)^3 : (0.516)^3 \cong 0.83 : 1$$

$$\text{Total active carrier source/drain dosage} = \text{Dose (In)} + \text{Dose (B)}$$

For B and group III In and group V Sb combination:

Atomic radii of the atoms are: $R_{In} = 1.44 \text{ \AA}$, $R_{Sb} = 1.40 \text{ \AA}$, $R_{Si} = 1.11 \text{ \AA}$, $R_B = 0.8 \text{ \AA}$

$$R_{Si} = C * R_{In} + C * R_{Sb} + (1 - 2C) * R_B$$

$$C = 0.25$$

$$\text{Dose (In)} : \text{Dose (Sb)} : \text{Dose (B)} \cong 1 : 1 : 8$$

$$\text{Total active carrier source/drain dosage} = \text{Dose (In)} + \text{Dose (Sb)} + \text{Dose (B)}$$

[0024] After completion of the source/drain and strain compensation implants, a rapid temperature anneal (RTA) process may be performed to activate the dopants. The RTA process may be performed at a temperature of between about 600°C and about 1000 °C, for a time period of up to 5 seconds. Of course, one of ordinary skill in the art will appreciate that these parameters may vary depending upon the desired dopant profile.

[0025] A conventional nickel silicide process (e.g., deposition of thin Ni films on the stress relieved source/drain regions 170a, 170b followed by a RTA process is performed to form conductive NiSi films 180a and 180b over the source/drain regions 170a, 170b as illustrated in FIG. 1C. Because the tensile stresses in the source/drain regions of the substrate have been reduced, the NiSi films 180a and 180b formed at these regions will be enhanced, i.e., at or close to a single phase of 100 % pure NiSi. Hence, the formation of undesirable $NiSi_2$ at the source/drain regions will be substantially reduced or eliminated.

[0026] FIGS. 4A-4C are sectional views illustrating an alternate method of fabricating a PMOS semiconductor device according to the present invention. As illustrated in FIG. 4A, this method starts with a single crystal Si substrate 220 (or any substrate containing Si) including a gate structure 230 formed by a gate oxide 232 and a gate conductor 234, spacers 260a and 260b, source/drain regions 270a and 270b.

[0027] In accordance with the present invention, a layer 271 of amorphous Si (a-Si) is deposited over the source/drain regions 270a and 270b, or partially replaces the source/drain regions 270a and 270b, i.e., the top portions of the source/drain regions 270a and 270b become amorphous after this process. In some embodiments, an additional amorphization implant followed by an RTA process may then be performed to maintain the source/drain regions 270a and 270b. The a-Si layer 271 may also be formed over the source/drain regions 270a and 270b during the source/drain implantation process, i.e., the source/drain implantation typically results in the formation of an a-Si layer which is recovered by RTA or may be formed by an additional amorphization implantation right before nickel film deposition. The thickness of the a-Si layer 271 may be adjusted to a desired thickness by an appropriate implantation conditions such as dopants, dose, energy, temperature and current. The desired thickness of the amorphous layer may also be achieved by reducing the anneal temperature of the subsequent source/drain dopant activation RTA process, as illustrated in FIG. 4B. The reduced anneal temperature partially crystallizes the a-Si layer 271 up from the Si substrate side, thereby reducing the thickness of the a-Si layer 271 on the surface of the substrate to the desired thickness. In one embodiment, the reduced anneal temperature may be about 700 °C (reduced from a typical ~1000 °C anneal temperature). The desired thickness of the a-Si layer 271

depends upon the thickness of the nickel film to be deposited further on during silicidation, as the nickel films will consume a certain percentage of the a-Si layer 271 to form NiSi. Typically, a nickel film of a given thickness will consume an a-Si layer of 1.8 times of the given thickness during silicidation to form NiSi. Therefore, in a typical embodiment of the invention, the ratio of the thickness of the Ni films to the desired thickness of the a-Si layer may be about 1:1.8.

[0028] FIG. 4C illustrates the silicidation process described immediately above which forms NiSi films 280a and 280b over the source/drain regions 270a, 270b. Silicidation may be performed using conventional RTA parameters for nickel silicide. Generally, the silicidation process only consumes the remaining portion of the a-Si layer. Thus, the NiSi films 280a and 280b formed at the source/drain regions are enhanced because the stress induced formation of undesirable NiSi₂ at the source/drain regions has been substantially prevented by use of the a-Si layer 271 during silicidation (as long as layer 271 is a-Si substrate, the stress will not impact the silicide formation as it does single crystal Si).

[0029] FIGS. 5A-5C are sectional views illustrating another method of fabricating a PMOS semiconductor device according to the present invention. As illustrated in FIG. 5A, this method starts with a single crystal Si substrate 320 (or any substrate containing Si) including a gate structure 330 formed by a gate oxide 332 and a gate conductor 334, spacers 360a and 360b and source/drain regions 370a and 370b in the substrate.

[0030] In accordance with the present invention, an a-Si layer 371 is deposited over the substrate to a desired thickness, depending upon the thickness of the nickel film to be deposited further on during silicidation, as illustrated in FIG. 5B. The a-Si layer 371 may be deposited using a conventional chemical vapor deposition process. The desired

thickness of the a-Si layer 371 also depends upon the thickness of the nickel film to be deposited further on during silicidation, as discussed above in the previous embodiment. Therefore, in a typical embodiment of the invention, the ratio of the thickness of the Ni films to the desired thickness of the a-Si layer may be about 1:1.8.

[0031] FIG. 5C illustrates the silicidation process described immediately above which forms NiSi films 380a and 380b over the source/drain regions 370a, 370b. The silicidation may be performed using conventional RTA parameters for nickel silicide. As in the method of FIGS. 4A-4C, the silicidation process consumes the a-Si layer 371 instead of the tensile stressed epi-Si/single crystal Si, substrate. Consequently, the NiSi films 380a and 380b formed at the source/drain regions 370a, 370b are enhanced because the stressed induced formation of undesirable NiSi_2 at the source/drain regions has been substantially prevented by use of the a-Si layer 271 during silicidation.

[0032] FIGS. 6A-6C are sectional views illustrating still another method of fabricating a MOS semiconductor device according to the present invention. As illustrated in FIG. 6A, the method commences with the formation of a buried layer in a p-or n-type Si substrate or any substrate containing Si. The buried layer should have a lattice constant that is larger than the lattice constant of the Si. For example, buried layers composed of Ge, SiGe, or SiO_2 have lattice constants larger than Si. As illustrated in FIG. 6A, the buried layer may be formed by epitaxially growing the buried layer 421 on the substrate 420 and then forming a layer 422 of Si over the buried layer 421. The Si layer 422 may be formed using a conventional CVD process. Since the buried layer 421 has a lattice constant which is greater than Si, the Si layer 422 will be placed in stress

[0033] As illustrated in FIG. 6B, a gate structure 430, including a gate oxide 432 and a gate conductor 434, is formed over Si layer 422 followed by the formation of first and second non-conductive spacers 460a, 460b along opposing side walls of the gate structure 130. The gate structure 430 and spacers 460a, 460b may be similar to the gate and spacer structures described earlier with respect to FIG. 1A.

[0034] As further illustrated in FIG. 6B, a conventional source/drain implantation process may then be performed using a p-type dopant such as B and BF_2 to form self-aligned first and second p+ source/ drain regions 470a, 470b in the Si layer 422. Since the B atoms have atomic radii that are smaller than Si, the underlying buried film 421 compensates or nulls the tensile stresses caused by B implant or other process parameters

[0035] Conventional RTA and nickel silicidation processes may be performed to respectively activate the dopants and form conductive NiSi films 480a and 480b over the source/drain regions 470a, 470b as illustrated in FIG. 6C. Because the tensile stresses in the source/drain regions of the Si layer 422 have been substantially reduced or eliminated by the buried layer 422, the NiSi films 180a and 180b formed at these regions will be enhanced because the formation of undesirable NiSi_2 at the source/drain regions will be substantially reduced or eliminated. Even if a small quantity of undesired NiSi_2 is formed, the underlying buried layer 421 will prevent NiSi_2 from forming deeper below the depth of the buried layer.

[0036] FIGS. 7A-7C are sectional views illustrating yet another method of fabricating a MOS semiconductor device according to the present invention. As illustrated in FIG. 7A, the method may commence with a single crystal Si substrate 520 (or any substrate containing Si) including a gate structure 530 formed by a gate oxide 532 and a gate

conductor 534, dielectric spacers 560a and 560b, tensile-stressed p+ source/drain regions 570a and 570b in the substrate and nickel films 575a and 575b, for silicidation, disposed over the source/drain regions 570a and 570b, respectively.

[0037] As illustrated in FIG. 7B, dielectric capping layers 590a and 590b composed of nitride, oxide or oxynitride may be formed over the nickel films 575a and 575b, respectively. The dielectric spacers 560a and 560b and/or the dielectric capping layers 590a and 590b may be formed under tensile stress. The dielectric capping layers 590a and 590b should be composed of a material which places the Si substrate 575a and 575b in compression such as nitride. The compression provided by dielectric capping layers 590a and 590b compensates or nulls the tensile stresses in the underlying nickel films 575a and 575b.

[0038] As illustrated in FIG. 7C, a conventional RTA process may be performed to convert the nickel films 575a and 575b to NiSi films 580a and 580b, respectively. The RTA parameters such as temperature and duration and the thickness of the nickel films 575a and 575b and the thickness of the cap layers 590a and 590b and spacers 560 and 560b are adjusted as required to counter-act the tensile stresses in the source/drain regions 570a, 570b of the substrate 520.

[0039] Because the tensile stresses in the nickel films 575a and 575b have been substantially reduced by the counter-acting compressive stress applied by the cap layers 590a and 590b and /or spacers 560a and 560b (the source/drain extension is under the spacers), the formation of undesirable NiSi_2 at the source/drain regions during silicidation will be substantially reduced or eliminated. After silicidation, the cap layers 590a and

590b may be removed using a conventional removal process such as dry etching or wet etching.

[0040] FIGS. 8A-8C are sectional views illustrating yet another method of fabricating a PMOS semiconductor device according to the present invention. As illustrated in FIG. 8A, the method may commence with a single crystal Si substrate 620 (or any substrate containing Si) including a gate structure 630 formed by a gate oxide 632 and a gate conductor 634, spacers 660a and 660b, tensile-stressed p⁺ source/drain regions 670a and 670b in the substrate and nickel films 675a and 675b, for silicidation, disposed over the source/drain regions 670a and 670b, respectively.

[0041] A two cycle RTA process is then performed to convert the nickel films 675a and 675b to NiSi films. As illustrated in FIG. 8B, the first cycle of the RTA process is performed to convert the nickel films 675a and 675b to metal-rich silicide (Ni₂Si) films 676a and 676b. In one embodiment, the first cycle may be performed at a temperature ranging from about 200 °C to about 220 °C for about 10 seconds to about 20 minutes. The low temperature of the first RTA cycle prevents the formation of NiSi₂, which forms easily between about 250 °C and about 400 °C.

[0042] As illustrated in FIG. 8C, the second cycle of the RTA process is performed to convert the Ni₂Si films 676a and 676b to NiSi films 680a and 680b. In one embodiment, the second cycle of the RTA process may be performed at a temperature of about 375 to about 425 °C for about 10 to about 20 seconds. If desired, the second cycle of the RTA process can be implemented during the subsequent deposition of an etch stop layer, which is typically performed at a deposition temperature of about 400 °C.

[0043] FIGS. 9A-9C are sectional views illustrating yet another method of fabricating a PMOS semiconductor device according to the present invention. As will become apparent further on, this method of the invention may be used as a repair process when NiSi_2 has formed thereby causing higher contact resistance. As illustrated in FIG. 9A, the method may commence with a Si substrate 720 including a gate structure 730 formed by a gate oxide 732 and a poly-Si gate conductor 734, spacers 760a and 760b, source/drain regions 770a and 770b in the substrate 720, NiSi_2 films 777a and 777b disposed over source/drain regions 770a and 770b, an interlayer dielectric 781 disposed over the NiSi_2 films 777a and 777b and contact holes 782a and 782b etched through to respective NiSi_2 films 777a and 777b.

[0044] As illustrated in FIG. 9B, an additional Ni deposition is performed to form a layer 778 of Ni over the NiSi_2 films 777a and 777b. Typically, the thickness range of the additional nickel is about 20 angstroms to about 40 angstroms. A conventional RTA process is then performed to convert the NiSi_2 films 777a and 777b to a NiSi films 780a and 780b, and any unreacted Ni that may be remaining after RTA may then be conventionally removed, as illustrated in FIG. 9C.

[0045] While the foregoing invention has been described with reference to the above, various modifications and changes can be made without departing from the spirit of the invention. Accordingly, all such modifications and changes are considered to be within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, the method comprising the steps of:

 providing a substrate;

 doping a silicon or silicon containing region of the substrate with a first dopant, the first dopant creating a stress in the region;

 doping the region with a second dopant that reduces stress in the region caused by the first dopant, the region with the first and second dopants comprising a source/drain region; and

 forming a nickel mono-silicide film on the source/drain region.
2. The method according to claim 1, wherein the second dopant has atoms with an atomic radii greater than the atomic radius of the silicon atom.
3. The method according to claim 1, wherein the doping step using the first dopant is performed to reach a specified active carrier concentration.
4. The method according to claim 3, wherein the second dopant in the source/drain region reduces the stress of the silicon in the region while maintaining the specified active carrier concentration achieved by the first dopant.

5. The method according to claim 1, wherein the second dopant is selected from the group consisting of group II elements, group III elements, group IV elements, and combinations thereof.
6. The method according to claim 1, wherein prior to the nickel mono-silicide forming step further comprising the step of activating the first and second dopants in the source/drain region.
7. A method of fabricating a semiconductor device, the method comprising the steps of:
- providing a substrate;
 - doping a silicon or silicon containing region of the substrate with a dopant to form a source/drain region, the dopant inducing stress in the source/drain region;
 - forming a layer of amorphous silicon on the source/drain region, the layer of amorphous silicon having a thickness;
 - forming a nickel mono-silicide film on the layer of amorphous silicon.
8. The method according to claim 7, wherein the amorphous silicon layer is formed to a desired thickness.
9. The method according to claim 8, wherein the amorphous silicon layer is formed by one of an existing ion implantation and additional amorphization implantation.

10. The method according to claim 8, wherein the amorphous silicon layer is performed by an ion implantation process.
11. The method according to claim 10, wherein the dopant activating step crystallizes a portion of the amorphous silicon layer from a substrate side of the amorphous silicon layer.
12. The method according to claim 7, wherein the nickel mono-silicide film forming step consumes generally only the amorphous silicon layer.
13. The method according to claim 7, wherein the nickel mono-silicide film forming step is performed by forming a nickel film on the source/drain region and annealing the substrate.
14. The method according to claim 13, wherein the formation of the nickel mono-silicide film consumes generally only the amorphous silicon layer.
15. A method of fabricating a semiconductor device, the method comprising the steps of:
 - providing a substrate;
 - forming a buried layer within the substrate, the buried layer having a lattice constant selected to place a silicon or silicon containing region of the substrate in stress;

doping the region of the substrate with a dopant to form a source/drain region, the dopant nulling the stress caused by the buried layer;

forming a nickel mono-silicide film on the source/drain region.

16. The method according to claim 15, wherein the buried layer forming step is performed by forming the buried layer over the substrate and covering the buried layer with a layer of silicon or silicon containing material.

17. The method according to claim 16, wherein the lattice constant of the buried layer is greater than that of silicon.

18. A semiconductor device comprising:

a substrate;

a buried layer disposed within the substrate, the buried layer having a lattice constant selected to place a silicon or silicon containing region of the substrate in stress;

a dopant implanted within the region to form a source/drain region, the dopant nulling the stress caused by the buried layer;

a nickel mono-silicide film disposed on the source/drain region.

19. A method of fabricating a semiconductor device, the method comprising the steps of:

providing a substrate;

doping a silicon or silicon containing region of the substrate with a dopant to form a source/drain region, the dopant causing a tensile stress in the region of the substrate;

forming a nickel film on the region;

forming a capping layer on the nickel film, the capping layer being selected from a material that compresses the nickel film and the underlying region; and

converting the nickel film to a nickel mono-silicide film.

20. The method according to claim 19, further comprising the step of removing the capping layer.

21. The method according to claim 19, wherein the capping layer comprises a dielectric material.

22. The method according to claim 19, wherein the converting step is performed by annealing the substrate.

23. A method of fabricating a semiconductor device, the method comprising the steps of:

providing a substrate;

doping a silicon or silicon containing region of the substrate with a dopant to form a source/drain region, the dopant causing a tensile stress in the region of the substrate;

forming a nickel film on the region;

converting the nickel film to a Ni_2Si film; and

converting the Ni_2Si film to a nickel mono-silicide film.

24. The method according to claim 23, wherein the nickel film converting step is performed by annealing the substrate at a temperature less than 250°C .
25. The method according to claim 24, wherein the annealing is performed for about 30 seconds.
26. The method according to claim 23, wherein the nickel film converting step is performed by annealing the substrate at a temperature of about 200°C to about 220°C .
27. The method according to claim 26, wherein the annealing is performed for about 30 seconds.
28. The method according to claim 23, wherein the Ni_2Si film converting step is performed by annealing the substrate at a temperature of about 400°C .
29. The method according to claim 28, wherein the annealing is performed for about 2 seconds.
30. In a semiconductor device including a substrate having a source/drain region and a nickel bi-silicide containing film disposed on the source/drain region, a method of

converting the nickel bi-silicide containing film to a nickel mono-silicide film,

comprising the steps of:

forming a layer of nickel on the nickel bi-silicide containing film; and

annealing the substrate to convert the nickel bi-silicide containing film to a nickel mono-silicide film.

31. The method according to claim 30, wherein the annealing step is performed by a rapid temperature anneal.

32. The method according to claim 30, further comprising the step of removing any unreacted portion of the layer of nickel from the mon-silicide film.