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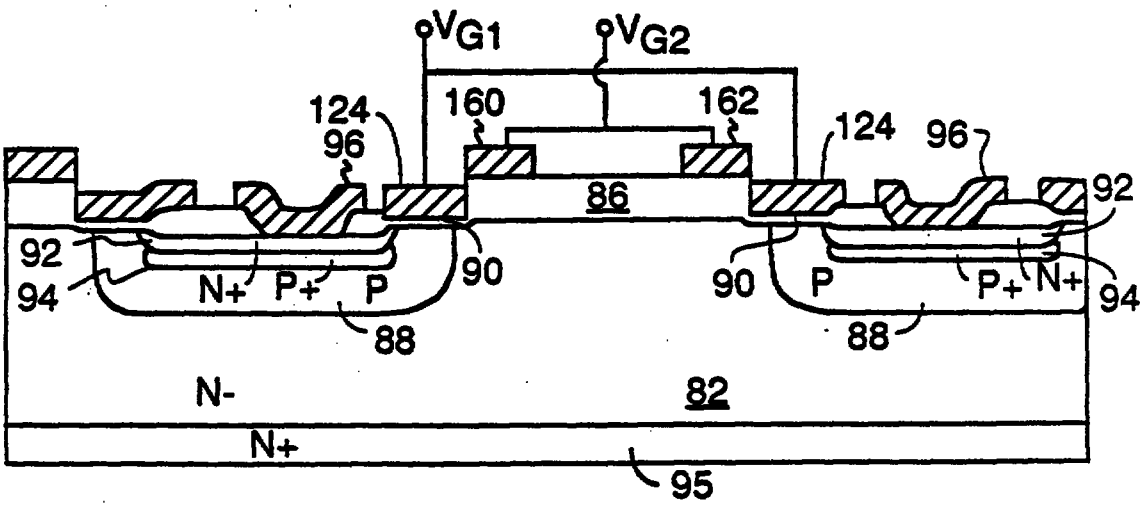
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(54) Title: MOSFET STRUCTURE HAVING REDUCED GATE CAPACITANCE AND METHOD OF FORMING SAME



(57) Abstract

In one embodiment, a vertical MOSFET is formed having a lower gate portion (124) overlying the channel region of the MOSFET and separated from the channel region by a thin gate oxide layer (90). An upper gate portion (120) is formed overlying the drain of the MOSFET and separated from the drain by a relatively thick oxide layer (86). In this particular embodiment, since the dielectric thickness between the upper gate portion (120) and the drain (82) is relatively large, the MOSFET exhibits a lower gate-drain capacitance (C_{GD}) value, while the threshold voltage of the MOSFET remains relatively unchanged. The upper gate portion (120) may be electrically connected to the lower gate portion (124) or may be electrically isolated from the lower gate portion (124). A preferred method of forming the resulting MOSFET having this lowered C_{GD} allows the source (92) and body regions (88) to be precisely aligned with the drain edge of the lower gate portion (124).

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