

ABSTRACTCLOCK SIGNAL GENERATION SYSTEM

5 A television receiver includes a phase-locked
loop (PLL) (226-232) which generates a clock signal (CLK)
having a frequency of N times the line frequency and being
phase-locked to the horizontal line synchronizing signal
(HSYNC). The clock signal produced by this PLL has a
10 frequency which tends to jitter between N+1 and N-1 times
the line frequency. To compensate for this jittering in
the frequency of the clock signal, phase alignment
circuitry (236) is coupled to the PLL to align the phase
of the clock signal to the horizontal drive signal (HD)
15 produced by the PLL on the occurrence of each horizontal
drive pulse. The PLL may also include a delay element
(234) which delays the horizontal drive signal applied to
the phase comparator of the PLL. This delay element
effectively advances the phase of the horizontal drive
20 signal and the line-locked clock signal with respect to
the horizontal sync signal to compensate for signal
processing delays imparted in the generation of the
horizontal drive signal and the clock signal.

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This Sheet Has Been Replaced