METHODS OF FORMING ISOLATED ACTIVE AREAS, TRENCHES, AND CONDUCTIVE LINES IN SEMICONDUCTOR STRUCTURES AND SEMICONDUCTOR STRUCTURES INCLUDING THE SAME

ABSTRACT

Methods of pitch doubling of asymmetric features and semiconductor structures including the same are disclosed. In one embodiment, a single photolithography mask may be used to pitch double three features, for example, of a DRAM array. In one embodiment, two wordlines and a grounded gate over field may be pitch doubled. Semiconductor structures including such features are also disclosed.

FIGURE 9