DESCRIPTION

METHODS OF FORMING A PLURALITY OF CAPACITORS

TECHNICAL FIELD

This invention relates to methods of forming a plurality of capacitors.

BACKGROUND OF THE INVENTION

Capacitors are one type of component commonly used in the fabrication of integrated circuits, for example in DRAM circuitry. A capacitor is comprised of two conductive electrodes separated by a non-conducting dielectric region. As integrated circuitry density has increased, there is a continuing challenge to maintain sufficiently high storage capacitance despite typical decreasing capacitor area. The increase in density of integrated circuitry has typically resulted in greater reduction in the horizontal dimension of capacitors as compared to the vertical dimension. In many instances, the vertical dimension of capacitors has increased.

One manner of fabricating capacitors is to initially form an insulative material within which a capacitor storage node electrode is formed. For example, an array of capacitor electrode openings for individual capacitors may be fabricated in such insulative capacitor electrode-forming material, with an example insulative electrode-forming material being silicon dioxide doped with one or both of phosphorus and boron. The capacitor electrode openings may be formed by etching. It can be difficult to etch the capacitor electrode openings within the insulative material, particularly where the openings are deep.

Further and regardless, it is often desirable to etch away most if not all of the capacitor electrode-forming material after individual capacitor electrodes have been formed within the openings. Such enables outer sidewall surfaces of the electrodes to provide increased area and thereby increased capacitance for the capacitors being formed. However, the capacitor electrodes formed in deep openings are often correspondingly much taller than they are wide. This can lead to toppling of the capacitor electrodes, either during the etch to expose the outer sidewalls surfaces, during transport of the substrate, and/or during deposition of the capacitor dielectric layer or outer capacitor electrode layer.

Our U.S. Patent No. 6,667,502 teaches the provision of a brace or retaining structure intended to alleviate such toppling. Other aspects associated in the formation of a plurality of capacitors, some of which include bracing structures, are also disclosed and are:

U.S. Published Application No. 2005/0051822;
U.S. Published Application No. 2005/0054159;
U.S. Published Application No. 2005/0158949;
U.S. Published Application No. 2005/0287780;
U.S. Published Application No. 2006/0014344;
U.S. Published Application No. 2006/0051918;
U.S. Published Application No. 2006/0046420;
U.S. Published Application No. 2006/0121672;
U.S. Published Application No. 2006/0211211;
U.S. Published Application No. 2006/0263968;
U.S. Published Application No. 2006/0261440;
U.S. Published Application No. 2007/0032014;
U.S. Published Application No. 2006/0063344;
U.S. Published Application No. 2006/0063345;

Fabrication of capacitors in memory circuitry may form an array of capacitors within a capacitor array area. Control or other circuitry area is often displaced from the capacitor array area, with the substrate including an intervening area between the capacitor array area and the control or other circuitry area. In some instances, a trench is formed in the intervening area between the capacitor array area and the other circuitry area. Such trench can be formed commensurate with the fabrication of the openings within the capacitor array area within which the isolated capacitor electrodes will be received.

When etching the insulative electrode-forming material within which the capacitor electrodes are received to expose outer sidewall surfaces thereof, it is often desired that none of the insulative material within the other circuitry area be etched. One prior art method restricts such by masking the peripheral circuitry area. Specifically, a silicon nitride layer may be formed over the predominantly insulative material within which the capacitor electrodes are

formed. The conductive material deposited to form the capacitor electrodes within the electrode openings also deposits and lines the trench between the capacitor array area and the peripheral circuitry area. One example conductive material is titanium nitride. The titanium nitride is polished back at least to the silicon nitride layer, thereby forming isolated container-shaped structures within individual capacitor electrode openings in the array area and within the trench. Accordingly, the sidewalls and bottom of the trench are covered or masked with titanium nitride, whereas the top or elevationally outermost surface of the peripheral or other circuitry area is covered with silicon nitride.

Etch access openings are then formed at spaced intervals within the silicon nitride within the capacitor array area to expose the insulative capacitor electrode-forming material therebeneath. Elevationally outermost surfaces of the peripheral circuitry area are typically kept entirely masked with the silicon nitride layer. When the insulative capacitor electrode-forming material comprises phosphorus and/or boron doped silicon dioxide, one example aqueous etching chemistry utilized to etch such highly selectively to titanium nitride and to silicon nitride is an aqueous HF solution. Such desirably results in exposure of the outer sidewalls of the individual capacitor electrodes while the peripheral insulative material remains masked from such etching by the overlying silicon nitride layer and from the titanium nitride within the peripheral trench.

Titanium nitride from which the capacitor electrodes are formed and which masks the sidewalls of the peripheral trench might be deposited in a manner which produces cracks or pinholes that extend laterally therethrough. This is not particularly problematic within the capacitor array area as it is desired that the insulative material be removed from both the inner and outer lateral sidewalls of the capacitor electrodes. Passage of liquid etchant through any cracks or pinholes within the array area does not defeat this purpose. However, cracks or pinholes in the titanium nitride layer protecting the lateral sidewalls of the peripheral circuitry insulative material can be problematic. Specifically, etchant seeping therethrough can cause etching voids or pockets to form laterally within the peripheral circuitry insulative material. These can later create fatal contact-to-contact shorts in the peripheral circuitry area when conductive vertical contacts are formed therein.

One existing solution to such problem is to deposit a very thin polysilicon layer to line internal portions of the capacitor electrodes and against the titanium nitride layer which laterally covers the insulative material of the peripheral circuitry area. Polysilicon is highly resistant to etch by HF. Such will shield any pinholes, thereby precluding HF or other etchants from seeping therethrough and undesirably etching the peripheral circuitry area insulative material.

Polysilicon is usually undesired subsequently, and is therefore removed. Accordingly, after etching back the insulative material to expose the outer sidewalls of the capacitor electrodes, a dedicated wet etch is conducted to highly selectively remove the polysilicon relative to undoped silicon dioxide, the titanium nitride, and the silicon nitride. Prior to this, a separate dedicated wet etch is conducted to remove an undesired native oxide which forms over the polysilicon.

Regardless of whether pinholes or cracks are formed in the capacitor electrode material, the material is often received against the silicon nitride, or other material, received over the insulative electrode-forming material. Such creates an interface or seam through which liquid etchant can seep which may undesirably cause etching of the insulative electrode-forming material in the periphery.

BRIEF DESCRIPTION OF THE DRAWINGS

Example embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic cross section of a substrate fragment in process in accordance with an aspect of the invention.

Fig. 2 is a diagrammatic top plan view of a larger scale portion of the Fig. 1 substrate.

Fig. 3 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1, and taken through line 3-3 in Fig. 4.

Fig. 4 is a diagrammatic top plan view of the Fig. 3 substrate fragment.

Fig. 5 is a view of the Fig. 3 substrate at a processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 5 substrate at a processing step subsequent to that shown by Fig. 5.

Fig. 6A is an enlargement of a portion of Fig. 6.

Fig. 7 is a view of the Fig. 6 substrate at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 7 substrate at a processing step subsequent to that shown by Fig. 7, and taken through line 8-8 in Fig. 9.

Fig. 9 is a diagrammatic top plan view of the Fig. 8 substrate fragment.

Fig. 10 is a view of the Fig. 8 substrate at a processing step subsequent to that shown by Fig. 8.

Fig. 11 is a view of an alternate processing of the Fig. 8 substrate to that depicted by Fig. 10.

Fig. 12 is a view of the Fig. 10 substrate at a processing step subsequent to that shown by Fig. 10.

Fig. 13 is a diagrammatic representation of DRAM circuitry.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example methods of forming pluralities of capacitors are described with reference to Figs. 1-13. Referring initially to Figs. 1 and 2, a substrate, for example a semiconductor substrate, is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Accordingly, and by way of example only, Fig. 1 might comprise a bulk semiconductor material (not shown), for example bulk monocrystalline, and/or comprise semiconductor-on-insulator layers.

Substrate 10 can be considered as comprising a capacitor array area 25, a circuitry area 75 other than capacitor array area 25, and an intervening area 50 between capacitor array area 25 and circuitry area 75. In the depicted example embodiment, intervening area 50 completely surrounds and encircles capacitor array area 25 (Fig. 2), and circuitry area 75 comprises a peripheral circuitry area to that of capacitor array area 25. Alternate constructions are contemplated, of course, for example whereby neither intervening area 50 nor circuitry area 75 completely or partially encircles a capacitor array area 25.

Fig. 1 depicts an insulative material 12 having electrically conductive storage node pillars 14 formed therethrough. Materials 12 and 14 may be fabricated over some suitable underlying material, for example bulk monocrystalline and/or underlying circuitry. Example insulative materials 12 include doped and undoped silicon dioxides, for example silicon dioxide deposited by the decomposition of tetraethylorthosilicate (TEOS) and/or borophosphosilicate glass (BPSG) and/or silicon nitride. Alternately by way of example only, material 12 might comprise anisotropically etched insulative sidewall spacers, for example formed about transistor gate lines (not shown). An example material 14 is conductively doped polysilicon. Conductive material 14 can be considered as comprising or defining a plurality of capacitor storage

node locations 15, 16, 17 and 18 on substrate 10. Storage node locations 15, 16, 17 and 18 are examples only, and regardless, may be conductive at this point in the process, or made conductive subsequently.

An example layer 22 has been formed over material 12 and capacitor storage node locations 15, 16, 17 and 18. Examples for layer 22 comprise silicon nitride and/or undoped silicon dioxide deposited to an example thickness range of from about 100 Angstroms to about 2,000 Angstroms. Layer 22 might be included to provide an etch stop, or other function.

Some insulative material 24 is received over capacitor array area 25 and circuitry area 75, and also in the depicted embodiment over intervening area 50. Such might be homogeneous or comprise multiple different compositions and/or layers. An example material is doped silicon dioxide comprising at least one of phosphorus and boron, for example BPSG, borosilicate glass (BSG), and/or phosphosilicate glass (PSG). An example thickness range for material 24 is from 5,000 Angstroms to 10 microns, with 2 microns being a specific example. Thinner and greater thicknesses are, of course, contemplated.

In one embodiment, a masking layer 26 (in one embodiment an insulator layer other than doped silicon dioxide) is received over insulative material 24. In some embodiments, such comprises, consists essentially of, or consists of silicon nitride. An example thickness range is from 200 Angstroms to 5,000 Angstroms. Some or all of layer 26 might be removed, or some or all of layer 26 might remain over the substrate as part of finished circuitry construction incorporating a plurality of capacitors being fabricated. Material other than silicon nitride might also be utilized, and not all embodiments of the invention necessarily require a masking layer 26.

Referring to Figs. 3 and 4, a plurality of capacitor electrode openings 28 has been formed within insulator layer 26, insulative material 24, and layer 22 over individual capacitor storage node locations 15, 16, 17 and 18. Further, a trench 30 has been formed in intervening area 50 within materials 26, 24 and 22. In one example embodiment, trench 30 completely surrounds capacitor area 25. An example technique for forming capacitor electrode openings 28 and trench 30 comprises photolithographic patterning and selective anisotropic dry etching to produce the example Figs. 3 and 4 constructions. An example minimum

width of trench opening 30 is from about 200 Angstroms to about 5,000 Angstroms, while an example minimum width for capacitor electrode openings 28 is from about 200 Angstroms to about 5,000 Angstroms. Trench 30 can be considered as comprising sidewall portions 31 and 33, and capacitor electrode openings 28 can be considered as having sidewall portions 27.

Referring to Fig. 5, conductive material 32 has been formed within capacitor electrode openings 28, and within trench 30 to line capacitor electrode openings 28 and trench 30 to less than completely fill trench 30. In the depicted example embodiment, conductive material 32 also less than fills capacitor electrode openings 28, and lines sidewalls portions 27 of capacitor electrode openings 28. Conductive material 32 can be considered as having inner sidewalls 40 and outer sidewalls 41 within capacitor electrode openings 28 within capacitor array area 25, and inner sidewalls 38 and outer sidewalls 39 within trench 30. An example conductive material 32 comprises titanium nitride deposited to an example thickness from about 20 Angstroms to about 1,000 Angstroms, with another example thickness being from about 200 Angstroms to about 300 Angstroms. Alternately, conductive material 32 might fill capacitor electrode openings 28. By way of example only where conductive material 32 comprises TiN, one manner of depositing such is by thermal chemical vapor deposition, for example at a substrate temperature of from about 450°C to about 680°C , a chamber pressure of from about 0.5 Torr to about 1.5 Torr, and using precursors comprising $TiCl_4$ and NH_3. Regardless, openings, cracks, and/or pinholes (not shown) may or may not be formed through some or all of the thickness of conductive material 32.

Referring to Figs. 6 and 6A, conductive layer 32 has been planarized back at least to an outer surface of insulator layer 26, thereby forming isolated/separate capacitor electrodes within capacitor electrode openings 28 and an isolation structure within trench 30. For purposes of the continuing discussion, conductive material 32 within trench 30 and insulative material 24 (which in the depicted embodiment also includes layer 26 thereover) can be considered as comprising an elevationally outer interface 37 therebetween.

Referring to Fig. 7, covering material 36 has been formed over insulator layer 26 and atop interface 37 and laterally over an upper portion of inner

sidewalls 38 of conductive material 32 within trench 30. In the depicted example embodiment, covering material 36 is also formed laterally over an upper portion of inner sidewalls 40 within capacitor electrode openings 28 within capacitor array area 25. In one embodiment, the upper portion of inner sidewalls 38 over which covering material 36 is formed is no greater than 20%, and in another embodiment no greater than 10%, of depth of trench 30 within insulative material 24, and/or 24/26/22 where layers 22 and 26 are present and are insulative. An example thickness range for layer 36 is from about 50 Angstroms to about 100 Angstroms over interface 37. Also in the depicted embodiment, covering material 36 does not laterally cover an entirety of inner sidewalls 38 of conductive material 32 within trench 30, and in one embodiment is deposited to be non-conformal over the upper portion of inner sidewalls 38 of conductive material 32 to have at least two different lateral thicknesses therealong. Regardless, in one embodiment, covering material 36 may or may not be formed onto a base portion of conductive material 32 within trench 30. For example, trench 30 can be considered as comprising a trench base 47, and conductive material 32 can be considered as being formed to have a portion 49 over and in contact with trench base 47. In the depicted example embodiment, none of covering material 36 is in contact with portion 49 of conductive material 32 that is over and in contact with trench base 47. Yet in other embodiments, some of covering material 36 may be formed in contact with portion 49 (not shown).

Covering material 36 may be formed to be of the same composition as that of an elevationally outermost portion of insulative material 22/24/26 (i.e., the same composition as material 26 in the depicted embodiment), or to be of different composition from that of an elevationally outermost portion of the insulative material. Further, covering material 36 might be formed to be any of one or a combination of insulative, conductive, and/or semiconductive. Example insulative materials include at least one of silicon nitride and undoped silicon dioxide. One example conductive covering material comprises W, for example in any of elemental, compound, and/or alloy forms. An example semiconductive material is polysilicon. Further and regardless, covering material 36 might comprise at least one of transparent carbon or amorphous

carbon. Regardless, covering material 36 might comprise multiple layers and/or materials and be deposited, by way of example only, by any suitable CVD and/or ALD process, and whether existing or yet-to-be developed.

Referring to Figs. 8 and 9, etch openings 45 have been formed through covering material 36 and insulator layer 26 within capacitor array area 25 effective to expose insulative material 24 within capacitor array area 25 while leaving elevationally outermost surfaces of insulative material 24 within circuitry area 75 completely covered with insulator layer 26 and covering material 36. Etch openings 45 provide access for liquid etchant to subsequently get to and etch material 24 within capacitor array area 25.

Referring to Fig. 10, insulative material 24 within capacitor array area 25 has been etched with a liquid etching solution effective to expose outer sidewall portions of outer sidewalls 41 of conductive material 32 within capacitor array area 25. The liquid etching solution during the etching of insulative material 24 may or may not also etch at least some of covering material 36 from substrate 10. Where the liquid etching solution during the etching of the insulative material also etches at least some of the covering material from the substrate, such might, by way of example only, etch less than 10% of the covering material from the substrate, etch at least a majority of the covering material from the substrate, or etch all of the covering material from the substrate. Fig. 10 depicts but one embodiment wherein the liquid etching solution has etched all of covering material 36 (not shown) from substrate 10. Fig. 11 depicts an alternate embodiment substrate 10a wherein the liquid etching solution during the etching of the insulative material has noticeably etched some, but not all, of covering material 36 from the substrate. Like numerals from the first described embodiment have been utilized where appropriate, with differences being indicated with the suffix "a". Accordingly, some of interface covering material 36 may or may not remain over the substrate at this point in the process, and/or in the resultant finished circuitry construction.

Where all of the covering material is etched from the substrate, such might be so completely etched prior to, in one embodiment, all of the insulative material that is etched by the liquid etching solution being etched from the substrate. In another embodiment, all of the interface covering material might

be etched from the substrate after all of the insulative material that is etched by the liquid etching solution is etched from the substrate. Where all of the covering material is etched from the substrate by the liquid etching solution, it is more desirable that all of the insulative material that will be etched by the liquid etching solution be completely etched from the substrate prior to such occurring of the covering material, for example to keep interface 37 thereby covered with some material 36 to preclude risk of liquid etchant seeping through interface 37, for example intending to minimize or eliminate material 24 within circuitry area 75 from being etched thereby.

An example liquid etchant solution is aqueous, and regardless for example comprising HF. One example solution comprises 5:1 to 20:1 water to HF by volume, wherein said HF is a 42 weight percent solution of HF in water. An example etching temperature is room ambient, with an example etching pressure also being room ambient. However, temperatures and pressures below and above room ambient are also contemplated. Additional example HF-containing solutions might contain any one or combination of HNO_3, acidic acid, NH_4F, and propionic acid. Liquid etchant solutions other than HF-containing are also contemplated.

By way of example only, a 10:1 by volume water to HF solution per the above can be used to etch PSG at a rate of approximately 5,000 Angstroms/minute to 15,000 Angstroms/minute, while etching an example covering layer consisting essentially of silicon nitride at a rate from 20 Angstroms/minute to 80 Angstroms/minute. Accordingly, covering layer 36 material and thickness may be selected and optimized in conjunction with the selection and modifying of etch conditions and etch times such that a desired amount of covering layer 36 is removed during etch-back to expose the outer surfaces of the capacitor electrodes, and in one embodiment with a degree of over-etch such that all of covering material 36 is removed without damaging etch of insulative material 24 received over circuitry area 75 by seeping action of liquid etchant along interface 37. Further considered, where covering material 36 comprises Si_3N_4 deposited by chemical vapor deposition, temperature at which such is deposited may impact density of the resultant layer and thereby resulting etch rate, for example in a HF solution. One embodiment,

for example where it may be desired to remove all of covering material 36 before or after example removal of material 24 within capacitor array area 25, comprises chemical vapor depositing Si_3N_4 at a temperature of at least 550°C to a thickness of from about 120 Angstroms to about 200 Angstroms. In another example embodiment, covering material 36 is formed at least in part by chemical vapor depositing Si_3N_4 at a temperature of no greater than 500°C to a thickness of from about 300 Angstroms to about 600 Angstroms.

One embodiment of a method of forming a plurality of capacitors contemplates forming conductive covering material atop interface 37 independent of whether such is formed laterally over an upper portion of sidewalls of conductive material 32 within trench 30, and if so regardless of whether conductive covering material does not laterally cover an entirety of inner sidewalls 38 of conductive material 32. Regardless thereof in such embodiment, the insulative material within the capacitor array area and the conductive covering material are etched with a liquid etching solution effective to expose outer sidewalls portions of the conductive material within the capacitor array area and to remove all of the conductive covering material from the substrate. Example materials, methods, and constructions are otherwise, for example, as described above.

Conductive material 32 within capacitor array area 25 is incorporated into a plurality of capacitors. For example, Fig. 12 depicts the deposition of a capacitor dielectric layer 60. By way of example only, an example material is a silicon dioxide, silicon nitride, silicon dioxide composite, or any suitable high k dielectric, whether existing or yet-to-be developed. By way of example only, high k dielectrics include Ta_2O_5 and barium strontium titanate.

An outer capacitor electrode layer 70 has been deposited over capacitor dielectric layer 60, thereby defining capacitors 81, 82, 83 and 84. Such are depicted as comprising a common cell capacitor plate to all of the depicted capacitors, for example as might be utilized in DRAM or other circuitry. For example and by way of example only, Fig. 13 depicts an example DRAM cell incorporating capacitor 81. Such comprises an example transistor gate wordline 87 having insulative sidewall spacers, an insulative cap and a conductive region under the cap such as a silicide, a conductive polysilicon

region under the silicide, and a gate dielectric region under the polysilicon. Source/drain regions 80 are shown formed within semiconductive material operatively proximate wordline 87. One of such electrically connects with capacitor 81, and another of such electrically connects with a bitline 85.

The above-described embodiment depicts at least some of layer 26 remaining as part of the finished circuitry construction. Further, any one or combination of the capacitor bracing structures referred to above in the "Background" section might be utilized. Alternately, no bracing might be utilized.

CLAIMS

The invention claimed is:

1. A method of forming a plurality of capacitors, comprising:

providing a substrate comprising a capacitor array area, a circuitry area other than the capacitor array area, and an intervening area between the capacitor array area and the circuitry area; an insulative material received over the capacitor array area and the circuitry area, the capacitor array area comprising a plurality of capacitor electrode openings within the insulative material received over individual capacitor storage node locations, the intervening area comprising a trench within the insulative material;

forming conductive material within the capacitor electrode openings and within the trench to line the capacitor electrode openings and the trench to less than completely fill the trench, the conductive material within the trench and the insulative material of the circuitry area having an elevationally outer interface laterally therebetween;

forming covering material atop the interface and laterally over an upper portion of inner sidewalls of the conductive material within the trench, the covering material not laterally covering an entirety of the inner sidewalls of the conductive material within the trench;

etching the insulative material within the capacitor array area with a liquid etching solution effective to expose outer sidewall portions of the conductive material within the capacitor array area; and

incorporating the conductive material within the capacitor array area into a plurality of capacitors.

2. The method of claim 1 comprising forming the covering material to be non-conformally deposited over the upper portion of the inner sidewalls of the conductive material to have at least two different lateral thicknesses therealong.

3. The method of claim 1 comprising forming the covering material to be of the same composition as that of an elevationally outermost portion of the insulative material.

4. The method of claim 1 comprising forming the covering material to be of different composition from that of an elevationally outermost portion of the insulative material.

5. The method of claim 1 comprising forming the covering material to be insulative.

6. The method of claim 5 comprising forming the covering material to comprise at least one of silicon nitride or undoped silicon dioxide.

7. The method of claim 1 comprising forming the covering material to be conductive.

8. The method of claim 7 comprising forming the covering material to comprise W.

9. The method of claim 1 comprising forming the covering material to be semiconductive.

10. The method of claim 9 comprising forming the covering material to comprise polysilicon.

11. The method of claim 1 comprising forming the covering material to comprise at least one of transparent carbon or amorphous carbon.

12. The method of claim 1 wherein the trench comprises a base, the conductive material being formed to have a portion over and in contact with the trench base, none of said covering material being in contact with said portion of conductive material that is over and in contact with the trench base.

13. The method of claim 1 comprising forming the covering material to a thickness of from about 50 Angstroms to about 1,000 Angstroms over the interface.

14. The method of claim 1 wherein the upper portion of the inner sidewalls over which the covering material is formed is no greater than 20% of depth of the trench within the insulative material.

15. The method of claim 1 wherein the upper portion of the inner sidewalls over which the covering material is formed is no greater than 10% of depth of the trench within the insulative material.

16. The method of claim 1 wherein the liquid etching solution during the etching of the insulative material also etches at least some of the covering material from the substrate.

17. The method of claim 16 wherein the liquid etching solution during the etching of the insulative material etches less than 10% of the covering material from the substrate.

18. The method of claim 16 wherein the liquid etching solution during the etching of the insulative material etches at least a majority of the covering material from the substrate.

19. The method of claim 16 wherein the liquid etching solution etches all of the covering material from the substrate.

20. The method of claim 19 comprising forming the covering material at least in part by chemical vapor depositing Si_3N_4 at a temperature of at least 550°C, the Si_3N_4 being deposited to a thickness of from about 120 Angstroms to about 200 Angstroms.

21. The method of claim 19 comprising forming the covering material at least in part by chemical vapor depositing Si_3N_4 at a temperature of no greater than 500°C, the Si_3N_4 being deposited to a thickness of from about 300 Angstroms to about 600 Angstroms.

22. The method of claim 19 wherein all of the insulative material that is etched by the liquid etching solution is etched from the substrate prior to all of the covering material being etched from the substrate.

23. The method of claim 19 wherein all of the covering material is etched from the substrate prior to all of the insulative material that is etched by the liquid etching solution being etched from the substrate.

24. The method of claim 1 wherein the insulative material comprises silicon dioxide comprising at least one of phosphorus and boron, and the liquid etching solution comprises HF.

25. A method of forming a plurality of capacitors, comprising:

providing a substrate comprising a capacitor array area, a circuitry area other than the capacitor array area, and an intervening area between the capacitor array area and the circuitry area; an insulative material received over the capacitor array area and the circuitry area, the capacitor array area comprising a plurality of capacitor electrode openings within the insulative material received over individual capacitor storage node locations, the intervening area comprising a trench within the insulative material;

forming conductive material within the capacitor electrode openings and within the trench to line the capacitor electrode openings and the trench to less than completely fill the trench, the conductive material within the trench and the insulative material of the circuitry area having an elevationally outer interface laterally therebetween;

forming conductive covering material atop the interface;

etching the insulative material within the capacitor array area and the conductive covering material with a liquid etching solution effective to expose outer sidewall portions of the conductive material within the capacitor array area and to remove all of the conductive covering material from the substrate; and incorporating the conductive material within the capacitor array area into a plurality of capacitors.

26. The method of claim 25 wherein the conductive covering material is formed laterally over an upper portion of inner sidewalls of the conductive material within the trench.

27. The method of claim 26 wherein the conductive covering material does not laterally cover an entirety of the inner sidewalls of the conductive material within the trench.

28. The method of claim 27 comprising forming the conductive covering material to be non-conformally deposited over the upper portion of the inner sidewalls of the conductive material to have at least two different lateral thicknesses therealong.

29. The method of claim 25 comprising forming the covering material to comprise W.

30. The method of claim 25 wherein the trench comprises a base, the conductive material being formed to have a portion over and in contact with the trench base, none of said conductive covering material being in contact with said portion of conductive material that is over and in contact with the trench base.

31. The method of claim 25 wherein all of the insulative material that is etched by the liquid etching solution is etched from the substrate prior to all of the conductive covering material being etched from the substrate.

32. The method of claim 25 wherein all of the conductive covering material is etched from the substrate prior to all of the insulative material that is etched by the liquid etching solution being etched from the substrate.

33. A method of forming a plurality of capacitors, comprising:

providing a substrate comprising a capacitor array area, a peripheral circuitry area other than the capacitor array area, and an intervening area between the capacitor array area and the peripheral circuitry area; a doped silicon dioxide material received over the capacitor array area and the peripheral circuitry area, an insulator layer other than doped silicon dioxide received over the doped silicon dioxide material within the capacitor array area and the circuitry area, the capacitor array area comprising a plurality of capacitor electrode openings within the insulator layer and the doped silicon dioxide material which are received over individual capacitor storage node locations, the intervening area comprising a trench within the insulator layer and the doped silicon dioxide material that completely surrounds the capacitor array area;

forming conductive material within the capacitor electrode openings and within the trench to line the capacitor electrode openings and the trench to less than completely fill the capacitor electrode openings and the trench, the conductive material within the trench and the insulator layer of the circuitry area having an elevationally outer interface laterally therebetween;

forming covering material over the insulator layer atop the interface and laterally over an upper portion of inner sidewalls the conductive material within the trench, the covering material not laterally covering an entirety of the inner sidewalls of the conductive material within the trench;

forming etch openings through the covering material and the insulator layer within the capacitor array area effective to expose the doped silicon dioxide material within the capacitor array area while leaving elevationally outermost surfaces of the doped silicon dioxide material within the peripheral circuitry area completely covered with the covering material and the insulator layer;

etching the doped silicon dioxide material within the capacitor array area through the etch openings with a liquid etching solution effective to expose outer sidewall portions of the conductive material within the capacitor array area; and

incorporating the conductive material within the capacitor array area into a plurality of capacitors.

34. The method of claim 33 wherein the liquid etching solution during the etching of the insulator layer also etches at least some of the covering material from the substrate.

35. The method of claim 33 comprising forming the covering material to be non-conformally deposited over the upper portion of the inner sidewalls of the conductive material to have at least two different lateral thicknesses therealong.