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Description

Method for producing a nonvolatile memory cell.

The invention relates to a method for producing a nonvolatile memory cell in an integrated circuit starting from a whole-area silicon layer on a dielectric.

Nonvolatile memory cells are EEPROMs and flash EEPROMs. The silicon layer may be monocrystalline, polycrystalline or amorphous silicon. The dielectric used is usually silicon dioxide, for example as gate oxide, or silicon nitride.

In the production of memory cells of this type, there is generally produced, in the course of the first method steps, a polysilicon layer for the following structuring on a dielectric. The desired structuring, in particular of transistor gates, is carried out by means of photolithography. The etching processes used in that case make very high requirements of the photoresist; the wet-chemical etching processes, in particular, produce relatively large, greatly varying undercuts and lead, in principle, to concave polysilicon edges which can be treated only with difficulty from the standpoints of production engineering and planarization.

In polysilicon etching processes, there is the risk that the gate oxide situated under the polysilicon may be damaged. Since, moreover, the selectivity between the polysilicon and the silicon oxide is insufficient during etching, in a manner dictated by the system, the gate oxide is thinned in an unreproducible manner outside the gate regions in the source/drain regions which are to be produced later, with the result that said gate oxide, for defined source/drain implantation, has to be completely removed and replaced by an oxide that is to be newly formed. This necessitates a further wet-chemical etching process.

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This last-mentioned etching produces a hollow groove in the gate oxide under the polysilicon gate edge, which produces a nonhomogeneous, difficult-to-control transition from the gate to the source/drain region with corresponding yield and reliability risks for the transistor. With regard to cleaning and to the oxidation behaviour, such a hollow groove can be controlled only with difficulty in terms of process engineering. In particular, the insulation strength of an insulation oxide, formed thereon, with respect to a second polysilicon layer, for example in an EEPROM process, is adversely influenced by this fact.

Furthermore, DE 27 39 662 A1 discloses, for the purpose of producing MOS transistors, covering the silicon layer with a layer which serves as oxidation protection, structuring the oxidation protection layer by means of photolithography in order to produce a mask by means of etching the oxidation protection layer and uncovering the polysilicon in the unmasked regions, and converting the polysilicon in the uncovered regions into silicon dioxide by means of local oxidation.

The invention is based on the object of specifying a simple method for producing a non-liquid memory cell.

This object is achieved by the fact that first of all the above-described method steps for producing the transistor are carried out and then

- a further polysilicon layer is applied, with inclusion of the remaining oxidation protection layer,

- a photoresist mask is applied and structured in such a way as to cover a region, situated above the field

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region, of the further polysilicon layer for forming the second electrode of the capacitor,

- the second electrode of the capacitor is produced by means of etching the second polysilicon layer in the unmasked regions, and

- if appropriate the oxidation protection layer is removed in the regions not required for the rest of the production process.

A basic concept of the invention may thus be seen in the fact that the structuring of the polysilicon, that is to say the removal of unnecessary polysilicon areas, is achieved not by conventional etching, but by conversion into silicon dioxide. The invention has the advantage that no gate oxide overetching and no associated hollow groove formation under the polysilicon edge arise, with the result that a homogeneous transition in the gate oxide from the gate region to the source/drain region is provided in the case of MOS transistors. Furthermore, the polysilicon side edge is completely embedded in a homogeneously grown oxide whose thickness corresponds approximately to at least that of the polysilicon. The insulation strength with respect to an optionally superior, second polysilicon layer, as in the case of an EEPROM, for example, is thereby determined only by the planar and therefore easy-to-control thickness of the nitride layer originally serving as structuring mask for the first polysilicon layer, or, if appropriate, of a different dielectric, since the limiting influence of the polysilicon edge is no longer present.

Furthermore, the invention avoids the disadvantage existing with conventional methods in the case of MOS transistors, whereby a process-dictated abrupt transition in the gate oxide thickness at the gate edge from the gate to the source/drain region

leads to a locally higher field strength between the gate edge and the source/drain region. Rather, a steady increase in the gate oxide thickness at the transition from the gate to the source/drain region is produced by the oxidation process. This avoids local field strength peaks with the consequence of amplified degradation of the transistor parameters in this critical region. The transistor reliability is increased in this way, in particular at higher operating voltages of the kind customary in EEPROM applications, for example.

Since the polysilicon edge produced by the oxidation according to the invention has a convex profile, this convex gate edge also contributes to avoiding the local field strength peaks and thus to better transistor reliability.

Furthermore, the invention achieves a sufficiently high breakdown voltage of the source/drain regions, which is very advantageous for example in EEPROM applications again. In combination processes, for example in the production of so-called embedded memories, it is therefore possible for source/drain regions of low-voltage logic transistors that are usually produced at a later point in time to be independently produced and optimized with fewer requirements on the dielectric strength. In the production of MOS transistors, it is advantageous that before the removal of the photoresist mask used during the photolithography, the source/drain implantation is effected through the uncovered silicon. The small doping gradient, which is responsible for the high breakdown voltage, of the source/drain diffusion for EEPROM applications, for example, is based on the fact that the implantation takes place relatively at the beginning of the entire production process and before the oxidation of the polysilicon which activates the implanted silicon dioxide and drives it into the silicon substrate.

The invention also avoids the disadvantage of conventional etching processes in which the system-dictated gaps between the polysilicon paths lead to planarization problems in the subsequent planes. They can only be resolved at great expense by means of deposition and etching back and also chemical mechanical polishing. In contrast, the invention has the advantage that between adjacent polysilicon paths there is a filling with silicon oxide which has been formed from the polysilicon at this location which has not been used in any case and is to be removed. Additional method steps for planarization can thus be obviated.

The invention also overcomes the disadvantage of conventional etching processes which, on the field oxide in those regions where the polysilicon has been removed, lead to a thinning of the field oxide and a corresponding decrease in the field oxide insulation properties. This loss then has to be compensated for by an increase in the field doping, but this in turn may have an adverse influence on certain transistor properties, such as breakdown and narrow width properties, for example, owing to the resulting increase in the doping gradient at the Locos edge. In contrast to this, the invention has the advantage that even in the field regions, unrequired polysilicon is converted into oxide, with the result that the field oxide thickness is increased there by the corresponding amount. The thickness increase corresponds essentially to the original polysilicon thickness. This results in an increase, if appropriate, in the threshold voltage of a parasitic field oxide transistor for the superior planes, such as the metallization layers, for example, or a possible second polysilicon plane.

A preferred design consists in the oxidation protection layer having at least one nitride layer.

Particularly good results are obtained by forming the nitride layer as an oxide-nitride (ON) sandwich or as an oxide-nitride-oxide sandwich layer (ONO layer) or as a nitrided oxide layer. Since all these masking layers may be very thin, it is also possible to etch them using simple wet-chemical agents with a tolerable size loss. Only low requirements are therefore made of the stability of the photoresist.

The invention is described in more detail below using an exemplary embodiment which is illustrated in the drawing, in which:

Figure 1 to Figure 4 each diagrammatically show a method step in the production of a transistor and of a capacitor as an EEPROM memory cell.

On a silicon substrate 1, a silicon oxide layer 2 is situated in the source/drain regions and between the field oxide.

According to Figure 1, a polysilicon layer 3 (poly1) is produced on the silicon oxide layer 2. Applied to said polysilicon layer is an oxide-nitride layer 4 (ON) and then a photoresist mask 5. The photoresist mask 5 corresponds to the desired polysilicon structures and leaves the source/drain regions free. The oxide-nitride layer 4 is then removed at the resist-free locations by means of an etching process, with the result that the polysilicon layer 3 is uncovered at these locations.

Immediately after the etching, and with the photoresist mask 5 being kept, according to Figure 2 implantation of the source/drain regions is carried out, using phosphorus in the example illustrated, through the uncovered polysilicon layer 3.

Subsequently, after the removal of the photoresist mask 5, according to Figure 3, the uncovered polysilicon is converted into silicon dioxide 7 by means of thermal oxidation

with correspondingly selected temperature/gas conditions, the oxide-nitride layer 4 with the structure produced according to Figure 1 serving as a mask. At the end of the oxidation, the resulting polysilicon edge has a convex profile. Moreover, during the oxidation, the implanted element 6 is activated and driven into the silicon substrate 1. After the end of the oxidation, the interspaces between the polysilicon structure are filled with thermal silicon dioxide and the polysilicon originally present is completely oxidized through at this point.

Even above the field regions 8, the unused polysilicon is converted into silicon dioxide 7, with the result that the field oxide thickness has increased there by somewhat more than an amount corresponding to the original polysilicon thickness. Furthermore, an oxide-nitride-oxide sandwich 9 has been produced from the oxide-nitride layer 4 by superficial oxidation of the nitride layer.

According to Figure 4, the production process is continued by applying a second polysilicon layer 10 in order to produce a capacitance between the first and second polysilicon layers 3, 10. A further photoresist mask 11 is applied to this above the capacitor region and structured. The photoresist mask 11 is used to produce the second polysilicon layer 10 as upper electrode of the desired capacitance. In this connection, Figure 4 reveals that the breakdown field strengths are determined only by the properties of the planar ONO layer 9. Furthermore, outside the active regions, the effective field oxide thickness is increased by the amount of this field oxide thickness.

Patent claims

1. A method for producing a nonvolatile memory cell having a transistor and a capacitor in an integrated circuit, in which case, starting from a whole-area silicon layer,

- the silicon layer is covered with an oxidation protection layer,

- the oxidation protection layer is structured by means of photolithography in order to produce a mask, which covers the gate region and a field region of the transistor, by means of etching the oxidation protection layer and uncovering the polysilicon in the unmasked regions, in such a way that the oxidation protection layer remaining over the field region forms the dielectric and the inferior polysilicon forms a first electrode of the capacitor

- the polysilicon in the regions that have been freed from the oxidation protection layer is converted into silicon dioxide by means of local oxidation, and

- a further polysilicon layer is applied, with inclusion of the remaining oxidation protection layer,

- a photoresist mask is applied and structured in such a way as to cover a region, situated above the field region, of the further polysilicon layer for forming the second electrode of the capacitor,

- the second electrode of the capacitor is produced by means of etching the second polysilicon layer in the unmasked regions, and

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- if appropriate the oxidation protection layer is removed in the regions not required for the rest of the production process.

2. The production method as claimed in claim 1, characterized in that the polysilicon conversion is effected by means of thermal oxidation.

3. The production method as claimed in claim 1 or 2, characterized in that the oxidation protection layer comprises at least one nitride layer.

4. The production method as claimed in claim 3, characterized in that the nitride layer comprises oxynitride or an oxide-nitride sandwich or an oxide-nitride-oxide.

5. The production method as claimed in one of claims 1 to 4,
characterized in that in the event of production of a MOS transistor, before the removal of the photomask used during the photolithography, the source/drain implantation is effected through the uncovered silicon.

6. The production method [lacuna] claim 5,
characterized in that the conversion of the polysilicon into silicon dioxide is effected in the source/drain regions and also the field oxide regions.

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