

Claims

1. A method for a channel encoding using a Low-Density Parity-Check (LDPC) code, the method comprising:
 - dividing information bits into a plurality of bit groups;
 - determining a number of information bits to be shortened;
 - determining a number of bit groups to be shortened based on the determined number of information bits to be shortened;
 - shortening information bits in the determined number of bit groups according to a predetermined order; and
 - LDPC encoding shortened information bits.
2. The method of claim 1, further comprising:
 - determining a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.
3. The method of claim 1, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-QAM.
4. The method of claim 1, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 4th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 3rd bit group, 11th bit group, 10th bit group, 9th bit group, 2nd bit group, 8th bit group, 7th bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 64-QAM.
5. The method of claim 1, comprising:
 - when a number of bits of each bit group is 360 and the information bits is 7200,
 - shortening all information bits in bit groups from 0th bit group to $(m-1)$ th bit group in the predetermined order; and
 - shortening $(7200-K_2-360m)$ information bits in m th bit group in the predetermined order,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200-K_2)$

is the number of information bits to be shortened, and $m = \left\lfloor \frac{7200-K_2}{360} \right\rfloor$.

6. An apparatus for a channel encoding using a Low-Density Parity-Check (LDPC) code, the apparatus comprising:

a parity-check matrix extractor for dividing information bits into a plurality of bit groups, determining a number of information bits to be shortened, determining a number of bit groups to be shortened based on the determined number of information bits to be shortened, and shortening information bits in the determined number of bit groups according to a predetermined order; and

LDPC encoder for LDPC encoding shortened information bits.

7. The apparatus of claim 6, wherein the shortening pattern applier is configured to determine a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

8. The apparatus of claim 6, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-QAM.

9. The apparatus of claim 6, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 4th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 3rd bit group, 11th bit group, 10th bit group, 9th bit group, 2nd bit group, 8th bit group, 7th bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 64-QAM.

10. The apparatus of claim 6, further comprising means for, when a number of bits of each bit group is 360 and the information bits is 7200, shortening all information bits in bit groups from 0th bit group to $(m-1)$ th bit group in the predetermined order; and shortening $(7200-K_2-360m)$ information bits in m th bit group in the predetermined order,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200-K_2)$

is the number of information bits to be shortened, and $m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$.

11. A method for a channel decoding using a Low-Density Parity-Check (LDPC) code, the method comprising:

demodulating a received signal;

determining position of shortened information bits; and

decoding the demodulated signal in consideration of the determined position of shortened information bits,

wherein determining position of shortened information bits comprises,

determining a number of information bits to be shortened; and

determining a number of bit groups to be shortened based on the determined number of information bits to be shortened; and

acquiring a predetermined order of bit groups.

12. The method of claim 11, wherein determining position of shortened information bits further comprising:

determining a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

13. The method of claim 11, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-QAM.

14. The method of claim 11, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 4th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 3rd bit group, 11th bit group, 10th bit group, 9th bit group, 2nd bit group, 8th bit group, 7th bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 64-QAM.

15. The method of claim 11, comprising:

when a number of bits of each bit group is 360 and the information bits is 7200,

determining that all information bits in bit groups from 0th bit group to (m-1)th bit

group in the predetermined order is shortened; and

determining that $(7200 - K_2 - 360m)$ information bits in m^{th} bit group in the predetermined order is shortened,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200 - K_2)$

is the number of information bits to be shortened, and $m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$.

16. An apparatus for a channel decoding using a Low-Density Parity-Check (LDPC) code, the apparatus comprising:

a demodulator for demodulating a received signal;

a shortening pattern determiner for determining position of shortened information bits; and

a decoder for decoding the demodulated signal in consideration of the determined position of shortened information bits,

wherein determining position of shortened information bits comprises,

determining a number of information bits to be shortened; and

determining a number of bit groups to be shortened based on the determined number of information bits to be shortened; and

acquiring a predetermined order of bit groups.

17. The apparatus of claim 16, wherein the shortening pattern applier is configured to determine a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

18. The apparatus of claim 16, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-QAM.

19. The apparatus of claim 16, wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 4th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 3rd bit group, 11th bit group, 10th bit group, 9th bit group, 2nd bit group, 8th bit group, 7th bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 64-QAM.

20. The apparatus of claim 16, further comprising means for, when a number of bits of each bit group is 360 and the information bits is 7200, determining that all information bits in bit groups from 0^{th} bit group to $(m-1)^{\text{th}}$ bit group in the predetermined order is shortened; and determining that $(7200-K_2-360m)$ information bits in m^{th} bit group in the predetermined order is shortened,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200-K_2)$

is the number of information bits to be shortened, and $m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$.

CLAIMS:

1. A method for channel encoding using a Low-Density Parity-Check (LDPC) code, the method comprising:

5 dividing information bits into a plurality of bit groups;
determining a number of information bits to be shortened;
determining a number of bit groups to be shortened based on the determined number of information bits to be shortened;

10 shortening information bits in the determined number of bit groups according to a predetermined order; and

LDPC encoding the shortened information bits,

wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

2. The method of claim 1, further comprising:

20 determining a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

3. The method of claim 1, comprising:

when a number of bits of each bit group is 360 and the information bits is 7200,

25 shortening all information bits in bit groups from 0th bit group to $(m-1)^{\text{th}}$ bit group in the predetermined order; and

shortening $(7200-K_2-360m)$ information bits in m^{th} bit group in the predetermined order,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200-K_2)$ is the

number of information bits to be shortened, and
$$m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor.$$

30 4. A method for channel decoding using a Low-Density Parity-Check (LDPC) code, the method comprising:

demodulating a received signal;

determining positions of shortened information bits; and

decoding the demodulated signal based on the determined positions of shortened information

35 bits,

wherein determining positions of shortened information bits comprises:

determining a number of information bits to be shortened; and

determining a number of bit groups to be shortened based on the determined number of information bits to be shortened; and

acquiring a predetermined order of bit groups,

wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

5. The method of claim 4, wherein determining position of shortened information bits further comprising:

10 determining a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

6. The method of claim 4, comprising:

when a number of bits of each bit group is 360 and the information bits is 7200,

15 determining that all information bits in bit groups from 0th bit group to $(m-1)$ th bit group in the predetermined order is shortened; and

determining that $(7200-K_2-360m)$ information bits in m th bit group in the predetermined order is shortened,

wherein, K_2 is a number of information bits to be obtained by shortening, $(7200-K_2)$ is the

20 number of information bits to be shortened, and
$$m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$$

7. An apparatus for channel encoding using a Low-Density Parity-Check (LDPC) code, the apparatus comprising:

25 a parity-check matrix extractor arranged to divide information bits into a plurality of bit groups, determine a number of information bits to be shortened, determine a number of bit groups to be shortened based on the determined number of information bits to be shortened, and shorten information bits in the determined number of bit groups according to a predetermined order; and

LDPC encoder arranged to LDPC encode the shortened information bits,

30 wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

35 8. The apparatus of claim 7, wherein the shortening pattern applier is configured to determine a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

9. The apparatus of claim 7, further comprising means for, when a number of bits of each bit group is 360 and the information bits is 7200, shortening all information bits in bit groups from 0th bit group to (m-1)th bit group in the predetermined order; and shortening (7200-K₂-360m) information bits in mth bit group in the predetermined order,

5 wherein, K₂ is a number of information bits to be obtained by shortening, (7200-K₂) is the number of information bits to be shortened, and

$$m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$$

10. An apparatus for channel decoding using a Low-Density Parity-Check (LDPC) code, the apparatus comprising:

10 a demodulator arranged to demodulate a received signal;
a shortening pattern determiner arranged to determine positions of shortened information bits;
and

a decoder arranged to decode the demodulated signal based on the determined positions of shortened information bits,

15 wherein the shortening pattern determiner determines the positions of shortened information bits by:

determining a number of information bits to be shortened; and
determining a number of bit groups to be shortened based on the determined number of information bits to be shortened; and

20 acquiring a predetermined order of bit groups,
wherein the predetermined order is 18th bit group, 17th bit group, 16th bit group, 15th bit group, 14th bit group, 13th bit group, 12th bit group, 11th bit group, 4th bit group, 10th bit group, 9th bit group, 8th bit group, 7th bit group, 3rd bit group, 2nd bit group, 1st bit group, 6th bit group, 5th bit group, 19th bit group, and 0th bit group, when a codeword length is 16200, the information bits is 7200, and a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

11. The apparatus of claim 10, wherein the shortening pattern applier is configured to determine a number of information bits to be obtained by shortening for determining the number of information bits to be shortened.

12. The apparatus of claim 10, further comprising means for, when a number of bits of each bit group is 360 and the information bits is 7200, determining that all information bits in bit groups from 0th bit group to (m-1)th bit group in the predetermined order is shortened; and determining that (7200-K₂-360m) information bits in mth bit group in the predetermined order is shortened,

35 wherein, K₂ is a number of information bits to be obtained by shortening, (7200-K₂) is the number of information bits to be shortened, and

$$m = \left\lfloor \frac{7200 - K_2}{360} \right\rfloor$$

13. A method for channel encoding, substantially as herein described with reference to Figures 6 to 14 of the accompanying drawings.

14. A method for channel decoding, substantially as herein described with reference to Figures 6 to 14 of the accompanying drawings.

15. An apparatus for channel encoding, substantially as herein described with reference to Figures 6 to 14 of the accompanying drawings.

10 16. An apparatus for channel decoding, substantially as herein described with reference to Figures 6 to 14 of the accompanying drawings.