WHAT IS CLAIMED IS:

[Claim 1]. A semiconductor device, comprising:

a string of transistors stacked in a vertical direction over a substrate of the semiconductor device having a channel structure extending in the vertical direction, the string of transistors including first, second and third substring of transistors that are arranged along first, second and third portions of the channel structure, respectively, the second substring of transistors being between the first substring of transistors and the third substring of transistors, wherein

gate structures of transistors in the first, second and third substring are separated by respective first, second and third insulating layers the second insulating layers have a higher etch rate than that of the third insulating layers, the string of transistors including a first discontinuity between critical dimensions (CDs) of the first and second portions of channel structure at a boundary between the first and second portions of the channel structure and a secondary discontinuity between CDs of the second and third portions of the channel structure and

of the first discontinuity and the second discontinuity are less than a threshold that is between 0.05 and 0.15.

[Claim 2]. The semiconductor device according to claim 1, wherein the first discontinuity between the CD at a bottom side of the second portion of the channel structure and the CD at a top side of the first portion of the channel structure is less than a threshold.

[Claim 3]. The semiconductor device according to claim 2, wherein the second discontinuity between the CD at a bottom side of the third portion of the channel structure

and the CD at a top side of the second portion of the channel structure is less than the threshold.

[Claim 4]. The semiconductor device according to claim 1, wherein a volumetric mass density of the second insulating layers is lower than that of the third insulating layers.

[Claim 5]. The semiconductor device according to claim 1, wherein a volumetric mass density of the second insulating layers is lower than a volumetric mass density of the first insulating layers.

[Claim 6]. The semiconductor device according to claim 5, wherein the second insulating layers are silicon oxide formed by a high density plasma chemical vapor deposition and the third insulating layers are silicon oxide formed based on tetraethoxysilane.

[Claim 7]. The semiconductor device according to claim 1, wherein a material composition of the second insulating layers is different from a material composition of the third insulating layers.

[Claim 8]. The semiconductor device according to claim 1, wherein a ratio of a number of transistors in the second substring over a sum of the number of transistors in the second substring and a number of transistors in the third substring is between 10 and 30%.

[Claim 9]. The semiconductor device according to claim 1, wherein the first insulating layers and the third insulating layers have an identical etch rate.