Claims

1. A semiconductor package comprising:

a first package interconnection component;

a second package interconnection component;

a first electrical component between the first package interconnection component and the second package interconnection component, the first electrical component having a first side and a second side opposite the first side;

a first bonding layer bonding the first side of the first electrical component and a first portion of the first package interconnection component;

a second bonding layer bonding the second side of the first electrical component and a first portion of the second package interconnection component;

a third bonding layer bonding a second portion of the first package interconnection component and a second portion of the second package interconnection component;

a second electrical component having a first side and a second side opposite the first side;

a fourth bonding layer bonding the first side of the second electrical component and the second portion of second package interconnection component;

a first heat sink;

a second heat sink;

a first interface layer bonding the first heat sink and the first package interconnection component;

a second interface layer bonding the second heat sink and the second package interconnection component;

a third package interconnection component;

a fifth bonding layer bonding the second side of the second electrical component and a first portion of the third package interconnection component so that the

second electrical component is between the second package interconnection component and the third package interconnection component; and

a sixth bonding layer bonding a second portion of the third package interconnection component and a third portion of the first package interconnection component.

2. The semiconductor package according to claim 1,

wherein the first electrical component is a power chip; and

wherein the second electrical component is a temperature sensor or a current sensor.

3. The semiconductor package according to claim 1,

wherein the first package interconnection component is a lead frame or a flexible printed circuit; and

wherein the second package interconnection component is a lead frame or a flexible printed circuit.

4. The semiconductor package according to claim 1,

wherein the second package interconnection component is bent to define the first portion, the second portion, and an intervening portion between the first portion and the second portion.

5. The semiconductor package according to claim 4,

wherein the intervening portion of the second package interconnection component is perpendicular to the first portion of the second package interconnection component, and also perpendicular to the second portion of the second package interconnection component.

6. The semiconductor package according to claim 1,

wherein the third package interconnection component is bent to define the first portion, the second portion, and an intervening portion between the first portion and the second portion.

7. The semiconductor package according to claim 6,

wherein the intervening portion of the third package interconnection component is perpendicular to the first portion of the third package interconnection component, and also perpendicular to the second portion of the third package interconnection component.

8. The semiconductor package according to claim 1,

wherein the first interface layer and the second interface layer comprise a dielectric material.

9. The semiconductor package according to claim 1, further comprising:

a mold encapsulation covering at least a portion of the first electrical component and at least a portion of the second electrical component.

10. The semiconductor package according to claim 1, further comprising:

one or more further electrical components between the first package interconnection component and the second package interconnection component.

11. The semiconductor package according to claim 10,

wherein the one or more further electrical components comprises a Schottky barrier diode.

12. A method of forming a semiconductor package, the method comprising:

bonding a first side of a first electrical component and a first portion of a first package interconnection component via a first bonding layer;

bonding a second side of the first electrical component, the second side of the first electrical component opposite the first side, and a first portion of a second package interconnection component via a second bonding layer so that the first electrical component is between the first package interconnection component and the second package interconnection component;

bonding a second portion of the first package interconnection component and a second portion of the second package interconnection component via a third bonding layer;

bonding a first side of a second electrical component and the second portion of second package interconnection component via a fourth bonding layer, the second electrical component also comprising a second side opposite the first side;

bonding a first heat sink and the first package interconnection component via a first interface layer;

bonding a second heat sink and the second package interconnection component via a second interface layer;

bonding the second side of the second electrical component and a first portion of a third package interconnection component via a fifth bonding layer so that the second electrical component is between the second package interconnection component and the third package interconnection component; and

bonding a second portion of the third package interconnection component and a third portion of the first package interconnection component via a sixth bonding layer.

13. The method according to claim 12,

wherein the first electrical component is a power chip; and

wherein the second electrical component is a temperature sensor or a current sensor.

14. The method according to claim 12,

wherein the first package interconnection component is a lead frame or a flexible printed circuit; and

wherein the second package interconnection component is a lead frame or a flexible printed circuit.

15. The method according to claim 12,

wherein the second side of the second electrical component is bonded with the first portion of the third package interconnection component before the first side of the second electrical component is bonded with the second portion of second package interconnection component.

16. The method according to claim 12,

wherein the first side of the second electrical component is bonded with the second portion of second package interconnection component before the second side of the second electrical component is bonded with the first portion of the third package interconnection component.

17. The method according to claim 12, further comprising:

forming a mold encapsulation to cover at least a portion of the first electrical component and at least a portion of the second electrical component.

18. The method according to claim 12, further comprising:

providing one or more further electrical components between the first package interconnection component and the second package interconnection component.