DMOS TRANSISTOR STRUCTURE & METHOD

ABSTRACT

An LDD lateral DMOS transistor is provided in a lightly-doped epitaxial layer of a first conductivity above a substrate of the same conductivity. A highly-doped buried layer of the first conductivity is provided under the LDD lateral DMOS transistor to relieve crowding of electrical equipotential distribution beneath the silicon surface. In one embodiment, a gate plate is provided above the gate and the gate-edge of the drift region. An optional N-well provides further flexibility to shape electric fields beneath the silicon surface. The buried layer can also reduce the electric field in a LDD lateral diode and improves cathode-to-anode reversed-recovery characteristics.

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