

ABSTRACT

A LOW TEMPERATURE RESIST TRIMMING PROCESS

A process is described for trimming photoresist patterns during the fabrication of integrated circuits for semiconductor devices and MEMS devices. A combination of a low temperature ($<20^{\circ}\text{C}$), high density oxygen and argon plasma and intense UV radiation is used to simultaneously trim and harden a photoresist linewidth in an ICP chamber. As an alternative, a UV hardening step can be performed in a flood exposure tool prior to the ICP plasma etch. Another option is to perform the argon plasma treatment first to harden the resist and then in a second step apply an oxygen plasma to trim the photoresist. Vertical and horizontal etch rates are decreased in a controllable manner which is useful for producing gate lengths in MOS transistors of less than 100 nm. The process can also be used to controllably increase a space width in a photoresist feature.

(No figure suitable for publication)

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