

Input circuit with accelerated switching.

The invention relates to a switching input circuit, comprising a stage of the emitter-coupled logic (ECL) type with two transistors, the first transistor receiving an input signal on its base and the second transistor receiving on its base a control signal which is generated by a control circuit from the signal from the collector of the first transistor in order to obtain on the collector of the second transistor an output signal switching faster than the input signal, the control circuit comprising a third transistor whose collector is connected to a supply voltage source, whose base is connected to the collector of the first transistor, and whose emitter is connected to a reference current source, referred to as the main current source, via an emitter resistor which is referred to as the first resistor.

Such a circuit, used in order to compensate for the slowing down in switching due to highly capacitive input lines, is known from the document JP-A-61-264909 (Patent Abstracts of Japan, Vol. 11, No. 117, (E-498), April 11, 1987, p. 159 E 498) in which the common junction between the emitter resistance and the main current source is connected to the base of the second transistor. When, for example, the voltage E changes from a low state to a high state, the turning on of the first transistor causes the lowering of the voltage on the base of the second transistor, which accelerates the switching. This phenomenon is the same, in the opposite direction, for a transition of the signal E from a high state to a low state. The direct interdependence of the control voltage and the signal from the collector of the first transistor means that it is not possible to select all of the operating parameters.

The present invention proposes an input circuit of the above-mentioned type in which the value and the amplitude of the control voltage can be selected.

This object is achieved in accordance with the invention by way of the means disclosed in Claim 1.

The invention will be better understood on reading the following description, given with reference to the sole figure which shows the preferred embodiment of the invention.

The circuit comprises an input follower stage comprising a transistor T_1 receiving on its base input signals e , and producing on an emitter signal E , said emitter being connected in a conventional way to a current source (T_2 , R_2). This buffer stage is conventional and has only an optional decoupling function. The actual input circuit
 5 comprises a gate of the emitter-coupled logic (ECL) type comprising two transistors T_3 and T_4 whose coupled emitters are connected to a current source (R_5 , T_5) of value I_1 . The collectors of the transistors T_3 and T_4 are connected to a supply voltage source V_c via the resistors R_3 and R_4 , respectively. The base of the transistor T_3 receives the signal E from the emitter of the transistor T_1 . The output signal S is the signal supplied
 10 by the collector of the transistor T_4 , the collector of the transistor T_3 supplying the complementary signal $\bar{S}$.

The base voltage of the transistor T_4 is determined by the collector voltage of the transistor T_3 .

The base of a transistor T_6 is connected to the collector of the transistor
 15 T_3 . The collector of the transistor T_6 is connected to a supply voltage V_c , and its emitter is connected to a point C via three resistors in series, R_{10} , R_{11} , and R_{12} respectively, a forward biased diode T_{10} possibly being interposed between the emitter of the transistor T_6 and the resistor R_{10} in order to perform a level compensation. The point A which is common to the resistors R_{10} and R_{11} is connected to a current source
 20 (R_8 , T_8) of value I_c . The point B which is common to the resistors R_{11} and R_{12} is connected to the base of the transistor T_4 , possibly via a resistor. The above-mentioned point C, at the other end of the resistor R_{12} , is connected to a reference voltage source U_{REF} . This reference voltage source comprises a transistor T_7 whose collector is connected to the supply voltage source V_c , whose base receives a reference voltage
 25 ($V_c - V_{REF}$), and an emitter of which is connected to the point C and to a current source (R_9 , T_9) of value I_D . This current I_D ensures, in particular, that a current I_R always flows through said emitter such that the following is always true:

$$U_{REF} = V_c - V_{REF} - V_{BE}$$

where V_{BE} denotes the base-emitter voltage of a transistor, being approximately 0.7V.

30 Three principal states can be distinguished. When the input signal E is at the low level (first state), the transistor T_3 is turned off and the collector of the transistor T_3 is at the voltage V_c . When the signal E is at the high level (second state),

the transistor T_3 is turned on and the collector of the transistor T_3 is at the voltage $V_c - \Delta V$, where:

$$\Delta V = R_3 I_1$$

This value ΔV of the switching amplitude is fixed by the standards

5 defining the circuit (800mV for ECL).

The third state is a state of transient equilibrium.

In the first state (E at the low level), the voltage on the emitter of the transistor T_{10} (point 0) is at the high level which is higher than the voltage at the point C and the entire current I_c passes through the resistor R_{10} . In the second state (E at the
10 high level), the voltage at the point 0 is at the low level which is lower than the voltage at the point C, the voltage at the point A is lower than that at the point C, and the current I_c is distributed between the two branches R_{10} and (R_{11}, R_{12}) . This enables control of the amplitude of the voltage variation on the base of the transistor T_4 and, therefore, the use of the input circuit for different values of ΔV . In the third state, the
15 voltage at the point A and at the point C are equal, no current flows in the branch (R_{11}, R_{12}) , and the voltage at the point B, therefore, has the value U_{REF} which must, for symmetrical operation, be equal to the value E_0 of the input signal E at mid-slope.

In this case the following is true:

$$E_0 = U_{REF} = V_c - V_{REF} - V_D$$

20 from which the value of V_{REF} is derived:

$$V_{REF} = V_c - V_D - E_0$$

There will now be described a method of calculating the components of the circuit which will enable a symmetrical operation to be obtained.

For a symmetrical operation, the circuit is chosen to be in the third state
25 for a switching half-amplitude, i.e.:

$$S = V_c - \frac{\Delta V}{2}$$

The equation of equilibrium is therefore written as:

$$V_c - \frac{\Delta V}{2} - V_D - V_{BE6} - R_{10} I_c = U_{REF} = V_c - V_{REF} - V_{BE7}$$

where V_D is the voltage drop in a diode

30 V_{BE6} is the base-emitter voltage of the transistor T_6

V_{BE7} is the base-emitter voltage of the transistor T_7 .

As the currents passing through the transistors T_6 and T_7 are respectively I_c and I_D , ($I_R = I_D$), the first condition is obtained:

$$R_{10}I_c = V_{REF} - \frac{\Delta V}{2} - V_D + V_T \log \frac{I_D}{I_c} \quad (1)$$

5 It is advantageous to choose $I_c = I_D$, giving:

$$R_{10}I_c = V_{REF} - \frac{\Delta V}{2} - V_D \quad (2)$$

giving:

$$R_{10}I_c = V_c - 2V_D - E_o - \frac{\Delta V}{2} \quad (2')$$

10 In the first state, the following is true (writing the equation of the voltages at the point A)

$$V_c - (V_{BE6} + V_D + I_{10}R_{10}) = V_c - V_{REF} - V_{BE7} + I_{11}(R_{11} + R_{12}),$$

I_{11} denoting the current passing through the resistors R_{11} and R_{12} . Thus,

$$V_{BE6} + V_D + I_{10}R_{10} + I_{11}(R_{11} + R_{12}) = V_{REF} + V_{BE7}$$

and

$$15 \quad I_{10} = I_c + I_{11}; I_{11} + I_R = I_D.$$

Thus:

$$V_{BE6} + V_D + (I_c + I_D - I_R)R_{10} + (I_D - I_R)(R_{11} + R_{12}) = V_{REF} + V_{BE7}$$

As the transistors T_6 and T_7 are traversed by currents which are equal to $I_c + I_D - I_R$ and I_R , respectively, the second condition is obtained:

$$20 \quad V_{REF} = V_T \log \frac{I_c + I_D - I_R}{I_R} + V_D + (I_c + I_D - I_R)R_{10} + (I_D - I_R)(R_{11} + R_{12})$$

The ratio n of I_D and I_R can be selected, for example equal to 2.

The following is then true for $n=2$ and $I_c = I_D$:

$$V_T \log 3 + V_D + \left(\frac{3}{2}R_{10} + \frac{R_{11} + R_{12}}{2} \right) I_c = V_{REF} \quad (4)$$

25 In the second state, the current I_{11} flows in the other direction and the current I_c is distributed between R_{10} on the one side and R_{11} and R_{12} on the other

side:

$$V_c - \Delta V - (V_{BE6} + V_D + I_{10}R_{10}) = V_c - V_{REF} - V_{BE7} - I_{11}(R_{11} + R_{12})$$

or:

$$\Delta V + V_{BE6} + V_D + I_{10}R_{10} = V_{REF} + V_{BE7} + I_{11}(R_{11} + R_{12}).$$

$$I_{10} + I_{11} = I_c$$

$$I_R = I_D + I_{11}$$

giving

$$V_{REF} = \Delta V + V_T \log \frac{I_c + I_D - I_R}{I} + V_D + (I_c + I_D - I_R)R_{10} + (I_R - I_D)(R_{11} + R_{12}) \quad (5)$$

where I_R has a value different from that in the first state.

The relationship $I_{11} = \frac{I_c}{2}$ is chosen, giving the third condition:

$$\Delta V + V_T \log \frac{I_c}{I_c + 2I_D} + V_D + \frac{R_{10} - (R_{11} + R_{12})}{2} I_c = V_{REF} \quad (6)$$

so for $I_c = I_D$:

$$\Delta V - V_T \log 3 + V_D + \frac{R_{10} - (R_{11} + R_{12})}{2} I_c = V_{REF} \quad (6')$$

The following expression is obtained on bringing together the equations

(4) and (6'):

$$(R_{10} + R_{11} + R_{12}) I_c = \Delta V - 2 V_T \log 3 \quad (7)$$

Using equation (2'), the following is obtained:

$$(R_{11} + R_{12}) I_c = \frac{3}{2} \Delta V - 2 V_T \log 3 - V_c + 2 V_D + E_o \quad (8)$$

The equations (2') and (8) enable the values of the components of the input circuit to be selected as a function both of the switching amplitude ΔV of the emitter-coupled stage and of the central switching value E_o on the base of the transistor T_3 .

It is furthermore possible to select the value of the deviation $|V_B - E_o|$ in the first and the second state. This deviation is the same in both these states because

a symmetrical function has been chosen (see above).

$$|V_B - E_0| = V_B - E_0 = V_c - 2V_D - \frac{3}{2}R_{10}I_c - \frac{R_{11}I_c}{2} E_0$$

Replacing $R_{10}I_c$ by its value taken from (2'), and replacing $V_c - E_0$ by $V_{REF} + V_D$, there is obtained:

$$5 \quad |V_B - E_0| = \frac{V_D}{2} + \frac{3}{4}\Delta V - \frac{V_{REF}}{2} - \frac{R_{11}I_c}{2} \quad (9)$$

By selecting the value of $R_{11}I_c$, the value of $|V_B - E_0|$ is selected and, therefore, the amplitude of the control signal.

Example:

$$\begin{aligned} V_{REF} &= 1.3 \text{ V} \\ 10 \quad \Delta V &= 600 \text{ mV} \\ I_c &= I_D = 250 \text{ } \mu\text{A} \\ V_D &= 0.75 \text{ V} \\ R_{10} &= 1 \text{ k}\Omega \\ R_{11} &= R_{12} = 500 \text{ } \Omega \\ 15 \quad |V_B - E_0| &= 112.5 \text{ mV} \end{aligned}$$

CLAIMS:

1. A switching input circuit, comprising a stage of the emitter coupled logic (ECL) type with two transistors, that is to say a first transistor (T_3) receiving an input signal on its base and a second transistor (T_4) receiving on its base a control signal which is generated by a control circuit from the signal from the collector of the first
5 transistor in order to obtain on the collector of the second transistor an output signal switching faster than the input signal, the control circuit comprising a third transistor (T_6) whose collector is connected to a supply voltage source (V_c), whose base is connected to the collector of the first transistor (T_3), and whose emitter is connected to a reference current source (I_c), referred to as the main current source, via an emitter
10 resistor (R_{10}) which is referred to as the first resistor, characterized in that the control circuit comprises a second resistor (R_{11}) and a third resistor (R_{12}) which are connected, in series with the first resistor (R_{10}), between the emitter of the third transistor (T_6) and a reference point (C) where to there are connected a reference voltage source (U_{REF}) and a reference current source (I_D), referred to as the auxiliary current source, the point (B)
15 common to the second resistor (R_{11}) and the third resistor (R_{12}) supplying the said control signal and being connected to the base of the second transistor (T_4).
2. A circuit as claimed in Claim 1, characterized in that the reference voltage source (U_{REF}) comprises a fourth transistor (T_7) whose collector is connected to the supply voltage source (V_c) and whose base is connected to a reference voltage
20 ($V_c - V_{REF}$).
3. A circuit as claimed in any one of Claims 1 or 2, characterized in that it comprises at least one forward biased diode (T_{10}) between the emitter of the third transistor (T_6) and the first resistor (R_{10}).