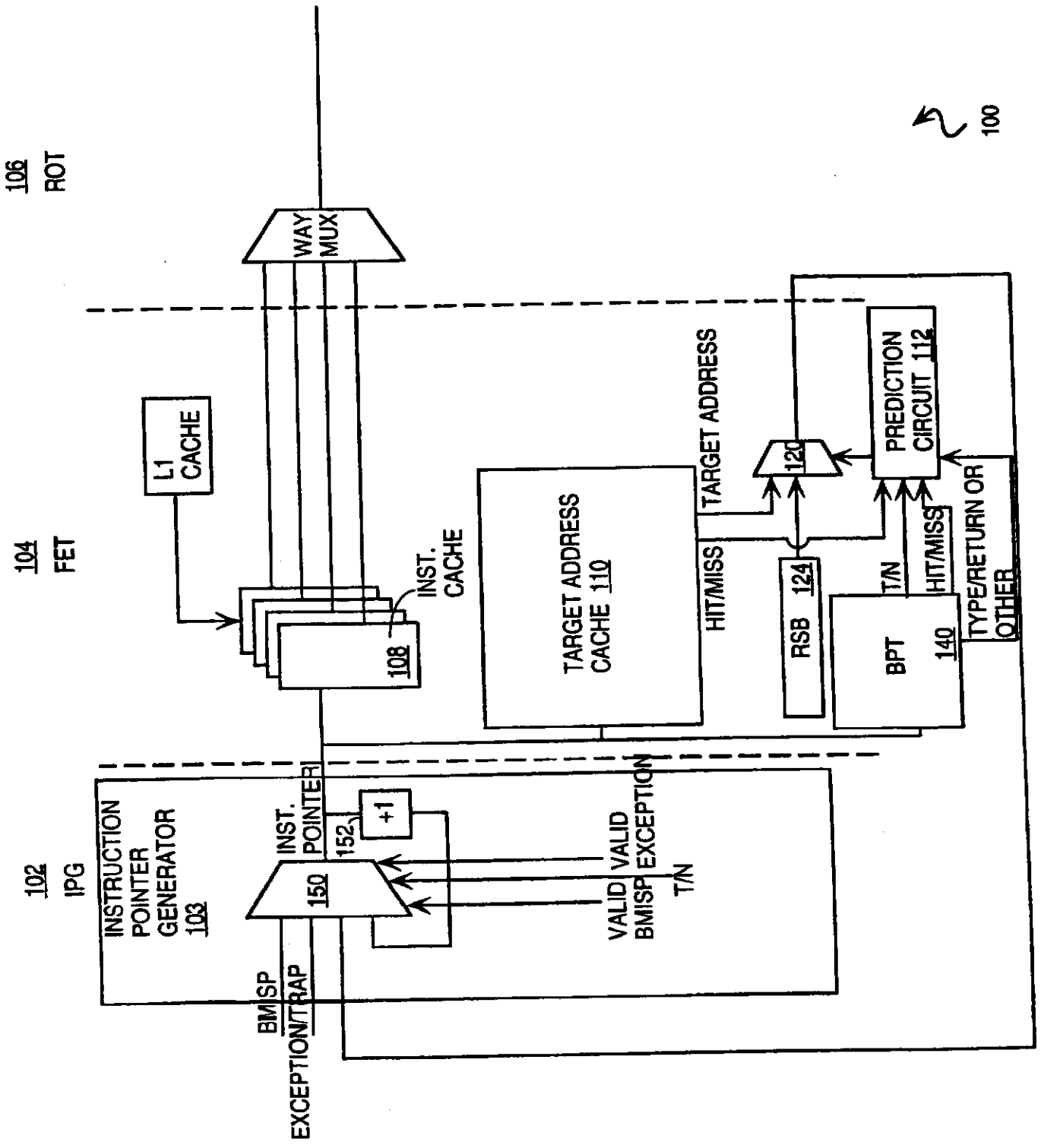
Fig. 1


100
106
ROT
WAY MUX
104
FET
L1 CACHE
INST. CACHE
108
TARGET ADDRESS CACHE 110
TARGET ADDRESS
HIT/MISS
120
PREDICTION CIRCUIT 112
RSB 124
BPT 140
T/N
HIT/MISS
TYPE/RETURN OR OTHER
102
IPG
INSTRUCTION POINTER GENERATOR 103
INST. POINTER
152
+1
150
VALID
BMISP
EXCEPTION
T/N
BMISP
EXCEPTION/TRAP

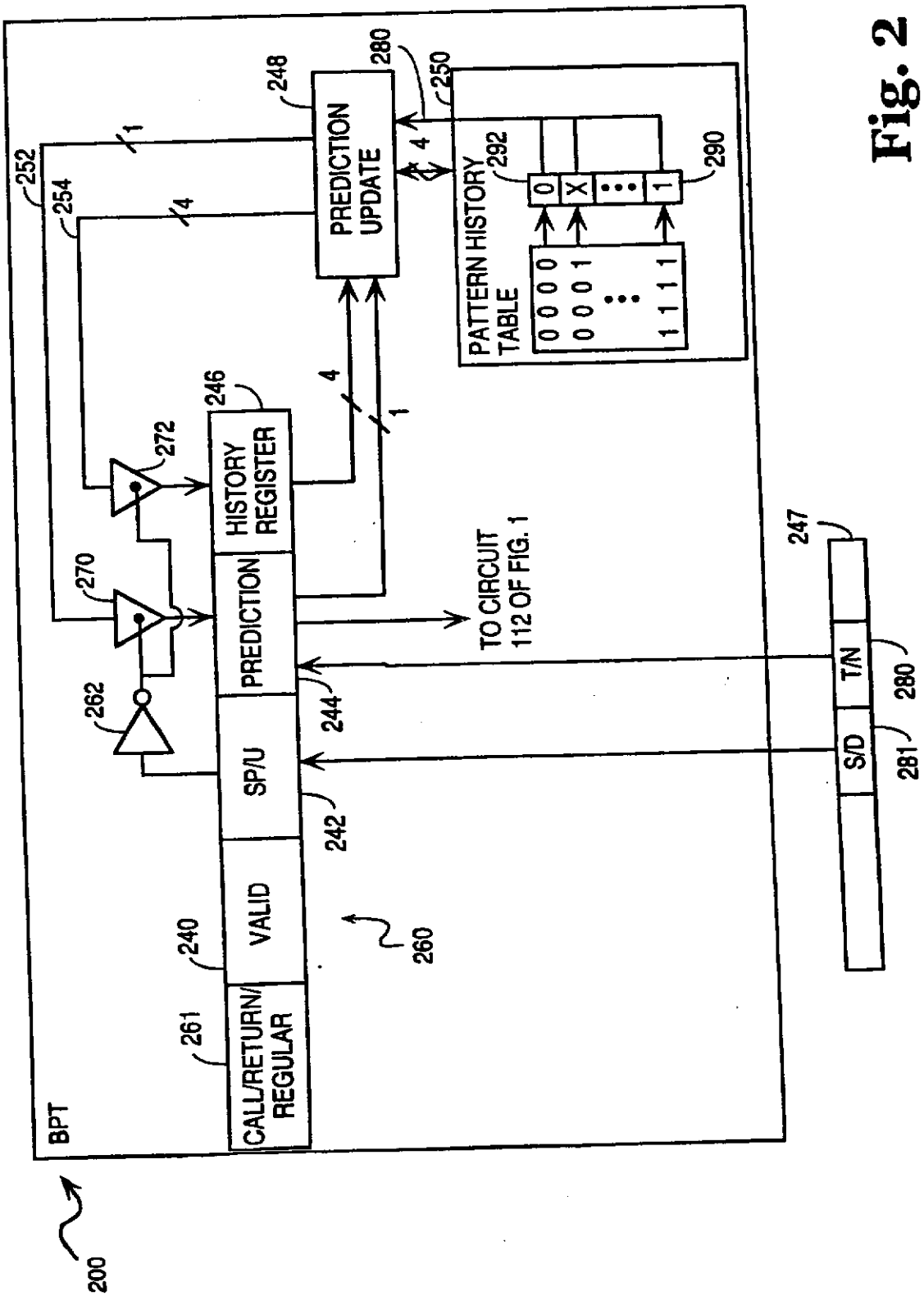

200
BPT
CALL/RETURN/ REGULAR
261
VALID
240
SP/U
242
PREDICTION
244
HISTORY REGISTER
246
PREDICTION UPDATE
248
PATTERN HISTORY TABLE
250
0 0 0 0
0 0 0 1
1 1 1 1
292
290
0
X
1
280
252
254
270
272
262
260
TO CIRCUIT 112 OF FIG. 1
247
T/N
S/D
281
280
1
4

Fig. 2

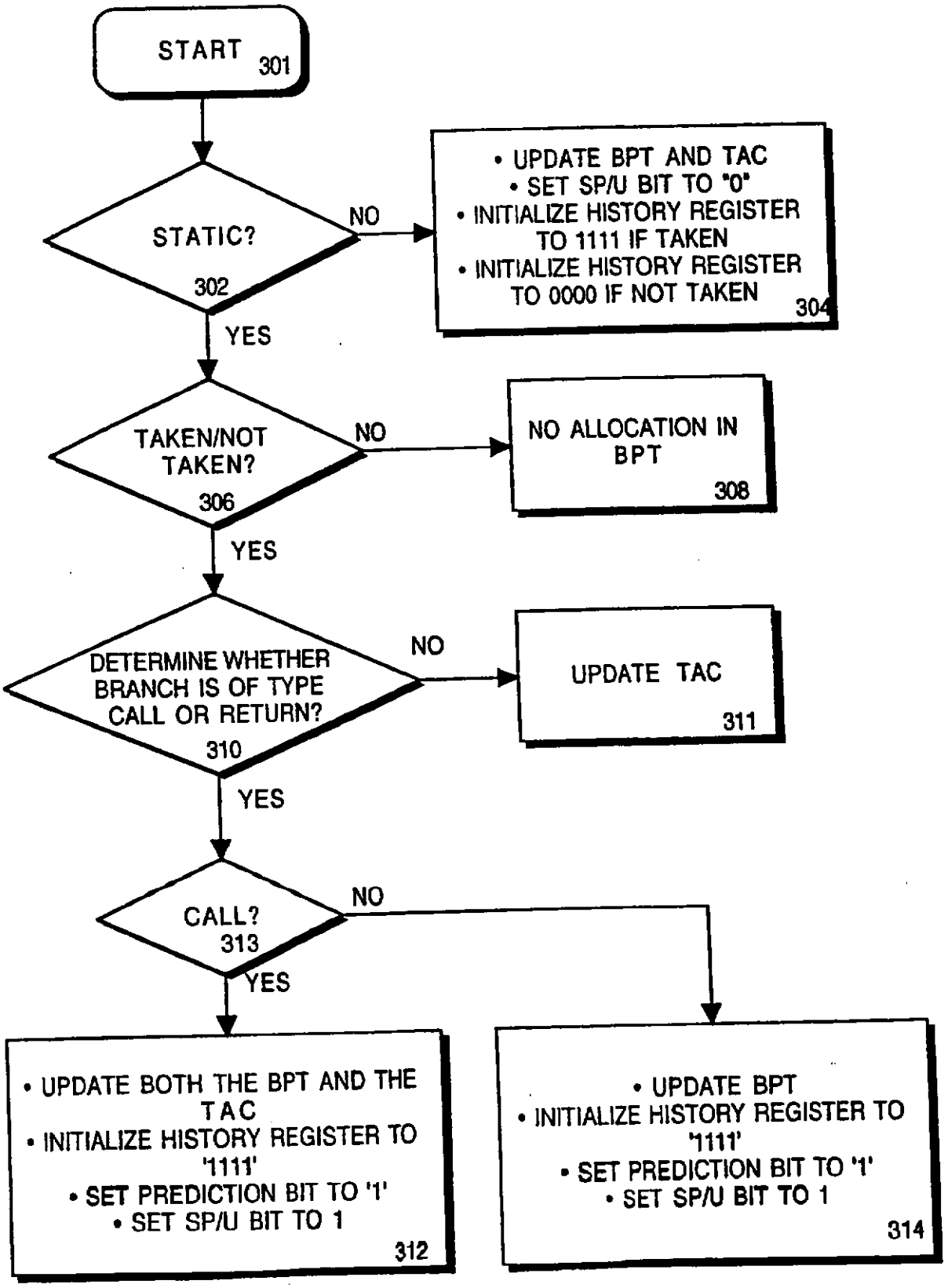

START
301
STATIC?
302
NO
• UPDATE BPT AND TAC
• SET SP/U BIT TO "0"
• INITIALIZE HISTORY REGISTER TO 1111 IF TAKEN
• INITIALIZE HISTORY REGISTER TO 0000 IF NOT TAKEN
304
YES
TAKEN/NOT TAKEN?
306
NO
NO ALLOCATION IN BPT
308
YES
DETERMINE WHETHER BRANCH IS OF TYPE CALL OR RETURN?
310
NO
UPDATE TAC
311
YES
CALL?
313
NO
YES
• UPDATE BOTH THE BPT AND THE TAC
• INITIALIZE HISTORY REGISTER TO '1111'
• SET PREDICTION BIT TO '1'
• SET SP/U BIT TO 1
312
• UPDATE BPT
• INITIALIZE HISTORY REGISTER TO '1111'
• SET PREDICTION BIT TO '1'
• SET SP/U BIT TO 1
314

Fig. 3