



DIGITAL/ANALOG CONVERSION OUTPUT CIRCUIT
HAVING AN OFFSET CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to a digital/analog conversion output circuit (also hereinafter called "D/A conversion output circuit"), and principally to a technology effective for use in an offset cancel technique for a D/A conversion output circuit installed in a modem (modulator/demodulator) provided in a portable communication terminal, for modulating and demodulating transmit and receive signals.

In a modem incorporated in a portable communication terminal, a modulating signal is outputted as an irreverse or non-inverse signal being in phase therewith and an inverse signal opposite in phase thereto. They are next inputted to a differential circuit of a high-frequency unit so as to cancel noise components and doubled so as to provide a satisfactory S/N (Signal-to-Noise Ratio). However, amplifier circuits for producing the non-inverse signal and the inverse signal, each of which comprises active elements, will normally cause offset voltages in some degree due to a variation in the manufacture of a semiconductor integrated circuit. If the offset voltages referred to above still remain, then innegligible noise and dc components are produced in a signal outputted from the differential circuit of the high-frequency unit.



Accordingly, the offset voltages have been standardized so as to fall below a predetermined value in the high-frequency unit. The offset control circuit and the portable communication terminal having it have been disclosed in Japanese Patent Application Laid-Open No. 6-303137, for example.

SUMMARY OF THE INVENTION

In the offset control circuit disclosed in the above-described publication, a non-inverse signal output and an inverse signal output are compared with their corresponding reference voltages (each corresponding to an analog middle voltage) to detect an offset, whereby an analog correction value and a digital correction value are outputted. This configuration will cause a problem in that since it is necessary to provide two pair of offset control circuits corresponding to amplifier circuits for producing the non-inverse signal and the inverse signal, the number of circuit elements increases.

An object of the present invention is to provide a D/A conversion output circuit capable of realizing its simplification and high-accuracy offset cancellation. The above and other objects, and novel features of the present invention will become apparent from the following description of the present specification and the accompanying drawings.

Typical ones of the inventions disclosed in the



present application will be summarized in brief as follows: In a digital/analog conversion output circuit comprising a digital/analog converter (also hereinafter called "D/A converter"), a first amplifier circuit for producing a non-inverse (output) signal being in phase with a signal outputted from the digital/analog converter, in response to the output signal, a second amplifier circuit for producing an inverse (output) signal opposite in phase to the output signal of the digital/analog converter in response to the output signal, offset voltages of the first and second amplifier circuits, each corresponding to an analog middle voltage are respectively detected and an average value digitized based on the detected values is added to a digital signal to be inputted to the digital/analog converter.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a block diagram showing one embodiment of a portable communication terminal equipped with a D/A



conversion output circuit having an offset control circuit according to the present invention;

Fig. 2 is a block diagram illustrating one embodiment of the offset control circuit shown in Fig. 1;

Fig. 3 is a block diagram depicting another embodiment of the offset control circuit shown in Fig. 1;

Fig. 4 is a schematic block diagram showing one embodiment of a majority circuit included in the offset control circuit shown in Fig. 1;

Fig. 5 is a circuit diagram showing one embodiment of a control circuit included in each of counter circuits shown in Figs. 2 and 3;

Fig. 6 is a potential distribution diagram for describing an offset cancel operation employed in the present invention;

Fig. 7 is a flowchart for describing a control operation of the offset control circuit shown in Fig. 1;

Fig. 8 is a timing chart for describing an offset detecting operation of the offset control circuit shown in Fig. 1; and

Fig. 9 is a schematic block diagram showing one embodiment of a high-frequency unit shown in Fig. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram showing one embodiment of a portable communication terminal equipped with a D/A conversion output circuit having an offset adjusting or



control circuit according to the present invention. The present portable communication terminal comprises a voice codec unit 100, a TDMA (Time Division Multiple Access) controller 200, a modem unit 300 and a high-frequency unit 400. The order of operations of these respective portions 100 through 400, the activation and/or deactivation of circuits and the like are controlled based on signals or pulses produced from a microcomputer 500, a regulator 600, a reset signal generating circuit 700 and a clock signal generating circuit 800.

The voice codec (coding/decoding) unit 100 suppresses a high-frequency noise component of a transmit analog voice signal inputted from a microphone with an unillustrated prefilter and converts it into a digital signal by an analog/digital converter (also hereinafter called "A/D converter) 101. A compressing circuit 102 band-compresses the digital signal in accordance with a digital signal process. In contrast to the above, an expanding circuit 103 expands the band-compressed digital signal corresponding to the received signal into its original band. A digital signal processor may be used to perform digital signal processing on these digital compressing/expanding operations. Further, a D/A converter 104 converts the expanded digital signal into a speech or voice analog signal and an unillustrated post filter suppresses a high-frequency component included in the converted output and amplifies its output so as to

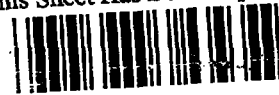


drive a speaker or the like.

The channel codec unit (TDMA controller) 200 performs the generation of codes for a time-division process and an error correction, an error check, an assembly and analysis of transmit and receive signal frames, for example so as to form a transmit or send signal SD (384Kbps) and a receive signal RD (384Kbps).

The modem unit 300 includes a waveform generating circuit 301 for performing modulation such as $\pi/4$ QPSK (Quadrature Phase Shift Keying) modulation suitable for radio transmission on the transmit signal SD outputted from the TDMA controller 200, a D/A converter 302 for converting an output produced from the waveform generating circuit 301 into an analog signal, a post filter 303 for suppressing a high-frequency component included in an output produced from the D/A converter 302, and an output buffer 304 for producing the irreverse or non-inverse and reverse or inverse signals. The output buffer 304 forms an I signal (non-inverse signal) and an IB signal (inverse signal) and a Q signal (non-inverse signal) and a QB signal (inverse signal) each composed of 96KHz, for example.

Contrary to the above, a received modulated signal IF is amplified by an amplifier 305. Further, phase information outputted from the amplifier 305 is first converted into a voltage by a phase detecting circuit 306 and a delay detecting circuit 307, which is next converted



into a digital signal by an A/D converter included in the delay detecting circuit 307, whereby the receive signal RD is formed.

The offset control circuit according to the present invention comprises an offset detecting circuit 309 and a correction circuit 310. As will be described later, the offset control circuit cancels a relative offset between non-inverse and inverse signals included in the output buffer.

The above-described phase modulation is normally often realized by a read-only memory ROM. The waveform generating circuit 301, the D/A converter 302 and the post filter 303, which serve as the phase modulator, are provided in parallel in the form of two pairs to obtain signals having a phase difference of 90° therebetween, i.e., signals crossing each other at right angles according to the I signal and the Q signal.

The high-frequency unit 400 eliminates in-phase noise components in response to the non-inverse and inverse signals outputted from the output buffer 304, i.e., a differential signal therebetween and cross-modulates the I and Q signals. Further, the high-frequency unit 400 modulates the resultant signal by a radio frequency carrier signal of 1.9GHz falling within a range from 800MHz to 2GHz, for example and amplifies it to predetermined transmit power so as to excite an antenna 232 through a transmit/receive changeover switch.



Moreover, the high-frequency unit 400 amplifies a signal received by the antenna 232 and the switch with an amplifier and frequency-converts the signal into an intermediate frequency IF of 10.8MHz, followed by sending to the input of the amplifier 305 of the modem unit 300.

A power supply switch SW is attached to a housing for the portable communication terminal. When the power supply switch SW is turned on prior to a telephone call of a speaker or caller, a power supply voltage supplied from a battery BAT mounted inside the portable communication terminal or from the outside of the portable communication terminal is supplied to each unit inside the portable communication terminal through the voltage regulator 600 or partially supplied directly to each unit as an operating voltage. Here, the voltage regulator 600 supplies a voltage value substantially constant to a change in voltage value due to the discharge or charge incident to the power consumption of the battery BAT to each unit inside the portable communication terminal.

The reset signal generating circuit 700 generates reset signals or the like for resetting data stored in registers of the respective units inside the portable communication terminal as needed when the power supply switch SW is in an on state. The clock signal generating circuit 800 generates a stable clock signal to be supplied to each unit inside the portable communication terminal and the microcomputer 500 for control. The clock signal



generating circuit 800 normally comprises a temperature-stabilized crystal oscillator and means for frequency-dividing or multiplying an output produced from the crystal oscillator. Although not illustrated in the drawing, a keypad, a dial signal generator, a call signal generator, etc. are provided in addition to the microcomputer 500, the reset signal generating circuit 700, the clock signal generating circuit 800, the power supply switch SW extending from the battery BAT and the voltage regulator 600.

The voice codec unit 100, channel codec unit 200, modem unit 300, high-frequency unit 400 and other electronic circuits, which constitute the portable communication terminal, are respectively configured so as to be able to provide a low source voltage operation and low power consumption. For instance, the voice codec unit 100 detects a voice silent state and stops the operation of a circuit principal part. Further, the modem unit 300 and the high-frequency unit 400 are configured so as to suppress power consumption by, for example, intermittently activating the circuit principal part using system configurational specs for providing radio calls in time-division multiplex form as well as to stop the operation of the circuit principal part at the time of the above silence. Such control is performed by detecting the states of the respective portions with the microcomputer 500.



In accordance with this, the offset control circuit according to the present invention is also activated by a predetermined control signal only upon turning on the power and resetting standby as will be described later. Only during a talking or traffic time after the completion of offset detection, a minimum of a plurality of registers and adders required to supply signals used for offset control are held under operating conditions, whereas other circuit portions are held in an inactive state so as to be incapable of operation.

Thus, the modem unit 300 most suitable for driving of the battery and the portable communication terminal equipped with the modem unit 300 can be realized. Namely, when the power is applied to the portable communication terminal so as to provide a power on/reset state and all the circuits or some circuits included in the modem unit 300 of the portable communication terminal are changed from a standby state for providing a non-call to a call or traffic set-up state capable of providing a call after power-on, the microcomputer 500 activates the respective component circuits of the offset control circuit so as to start an offset control operation of the offset control circuit.

After the commencement of the offset control operation, the microcomputer 500 maintains only a minimum of registers and adders of the respective component circuits in the offset control circuit at a state of being



capable of operation after the completion of a sequence of control operations for offset control and the offset control thereby to continuously generate an offset control signal. As a result, the unnecessary circuits are deactivated so that needless power consumption can be substantially restrained. Further, since the offset control signal becomes substantially unnecessary at the earliest when at least the modem unit 300 is changed to the standby state, it is needless to say that the microcomputer 500 brings all the circuits that constitute the offset control circuit, into a deactivated state.

An input/output circuit 308 installed in the modem unit 300 provides an interface between the modem unit 300 and the microcomputer 500. Although not restricted in particular, the microcomputer 500 supplies address signals used for various registers and memory circuits included in the modem unit 300 to the registers and memory circuits and inputs and output write or read data. A decoder included in the input/output circuit 308 forms a signal for selecting one register or memory circuit. Upon the above write operation, the write data is inputted to the corresponding one register or memory circuit. Upon the read operation, the data is held in the corresponding register or memory circuit and is outputted therefrom. The operations for control on the modem unit 300 by the microcomputer 500 include the above-described offset control operation, the setting of signal gain by the



amplifier 305 and the waveform generating circuit 301, etc.

Fig. 2 is a block diagram showing one embodiment of an offset control circuit according to the present invention. Respective circuit blocks illustrated in the same drawing are formed on a single semiconductor substrate together with the respective circuit blocks constituting the modem unit by the known semiconductor IC fabrication techniques.

A D/A converter, a filter and a differential output circuit shown in the same drawing correspond to the D/A converter 302, the post filter 303 and the output buffer 304 shown in Fig. 1. The differential output circuit comprises an unreversing or non-inverting amplifier circuit (+1) for producing a normal or non-inverse (output) signal identical in phase to a signal outputted from the filter, and a reverting or inverting amplifier circuit (-1) for producing an inverse (output) signal opposite in phase to the output signal of the filter (180° out of phase with the output signal thereof). Although not restricted in particular, these amplifier circuits (+1) and (-1) are comprised of differential amplifiers and respectively produce the above-described non-inverse and inverse signals each having a gain of 1. In this case, the amplifier circuits have an offset that even when an input signal is zero (ac middle voltage), an output voltage forms a positive or negative output signal with respect to the middle voltage due to the unbalance between



characteristics of a pair of elements in the differential circuit.

When such an offset voltage exists, the non-inverse (output) signal and the inverse (output) signal are inputted to the differential amplifier circuit of the high-frequency unit 400 shown in Fig. 1. Further, the differential amplifier circuit cancels noise components contained in both signals and doubles the signals so as to make an S/N ratio satisfactory. However, when the offset voltage referred to above occurs, innegligible noise and dc components are produced in the signal outputted from the differential circuit of the high-frequency unit. It is therefore necessary to cancel the offset produced between the amplifier circuits (+1) and (-1).

In the present embodiment, the circuits are commonly used to simplify the offset control circuit for canceling the above offset voltage. Namely, the non-inverse (output) signal of the amplifier circuit (+1) and the inverse (output) signal of the amplifier circuit (-1) are respectively selectively supplied to one input of a voltage comparator 21 through an analog switch 20. The other input of the voltage comparator 21 is supplied with a reference voltage V_{ref} produced by a reference voltage generating circuit 28. The reference voltage V_{ref} corresponds to the central value of the signal outputted from the D/A conversion output circuit, or the middle voltage of an analog signal.



A large or small compared output of the voltage comparator 21 is obtained as an up/down signal 1 and inputted to a majority circuit 22 although not restricted in particular. As will be described later, the majority circuit 22 time-sequentially takes in or captures the up/down signal 1 of the voltage comparator 21 in plural form in synchronism with the a majority clock signal. Next, a majority logical circuit LOG (shown in Fig. 4) in the majority circuit 22 makes a majority decision about such plural large and small compared outputs and produces an up/down signal 2 corresponding to each large or small compared output signal in accordance with the majority decision. The up/down signal 2 associated with such a large or small compared output is used for a count operation of +1 or -1 by a counter 23.

The counter 23 outputs either a true (non-inverse) output or a bar (inverse) output through a selector 2 for selecting either one of them and inputs it to an adder 1 through a selector 3 on the one side. The adder 1 is supplied with a DC code input signal via a selector 4. The DC code input signal is used as a digital signal corresponding to the central (middle) voltage of the analog signal.

Since the counter 23 is reset before the initiation of the offset cancel operation, the adder 1 outputs a digital signal corresponding to the DC code input signal upon commencement of the offset cancel operation and



inputs it to the D/A converter 302. The D/A converter 302 converts the DC code input signal into an analog signal and produces a voltage corresponding to the middle voltage through the filter 303. Accordingly, the first amplifier circuit (+1) of the differential output circuit forms a positive-phase or non-inverse output corresponding to the middle voltage. The signal outputted from the amplifier circuit (+1) is obtained by superimposing the input middle voltage and an offset voltage held by the amplifier circuit, itself on each other.

The analog switch 20 selects, for example, the signal outputted from the amplifier circuit (+1) and compares it with the above-described reference voltage V_{ref} . If the output signal of the amplifier circuit is larger than the reference voltage V_{ref} , then a low-level output signal (down signal) is produced. If the majority circuit 22 judges or determines the output signal as the down signal, then the counter 23 performs the -1 count operation. The counted output of -1 is inputted to the adder 1 through the selectors 2 and 3. Thus, a digital signal obtained by adding -1 to the DC code input signal is formed with respect to the result of the first comparison operation and thereafter the D/A conversion operation is performed again by the D/A converter 302. Since the digital signal $D1$ inputted to the D/A converter 302 is reduced by -1 as described above, the input (voltage) signal supplied to the input of the differential output circuit is reduced.



A voltage compare operation similar to the above is effected on the thus-lowered input voltage signal. If the output signal of the amplifier circuit (+1) is still larger than the reference voltage V_{ref} even if the input voltage signal is lowered, then the low-level output signal (down signal) is produced again. If the majority circuit determines the output signal as the down signal in the same manner as described above, then the counter 23 performs the -1 count operation. As a result, the total counted value becomes -2 (represented in the decimal numbering system to provide easy understanding of the invention) and serves so as to reduce the digital signal inputted to the D/A converter through the adder 1. Subsequently, the voltage comparator 21 repeatedly performs the operation similar to the above until the value of the input signal voltage becomes smaller than the reference voltage V_{ref} . As a result, a digital signal corresponding to the offset voltage of the amplifier circuit (+1) is formed by the counter 23.

If it is found at the first compare operation that the output signal of the amplifier circuit is smaller than the reference voltage V_{ref} , then a high-level output signal (up signal) is produced. If the majority circuit determines the output signal as the up signal, then the counter 23 performs the +1 count operation. The resultant counted output of +1 is inputted to the adder 1 through the selectors 2 and 3. Thus, a digital signal obtained by



adding +1 to a DC code input signal is produced with respect to the result of the first compare operation and the D/A converter 302 performs the D/A conversion operation again. Since the digital signal D1 inputted to the D/A converter 302 is increased by +1 upon the second compare operation as described above, the input voltage supplied to the input of the differential output circuit is rendered high. Thereafter, the voltage comparator repeatedly performs the same operation as described above until the input voltage becomes larger than the reference voltage V_{ref} . As a result, a digital signal associated with the offset voltage of the amplifier circuit (+1) is produced in the counter 23.

When the analog switch 20 is changed over to select the inverse output of the amplifier circuit (-1), the offset voltage of the amplifier circuit (-1) can be detected in the same manner as described above. However, since the amplifier circuit (-1) is used to form the inverse output, the polarity of the voltage developed in the output signal is reversed even if the offset voltage is the same. When up or down counting is made by the same voltage comparator and majority circuit, the polarity of the resultant voltage is reversed. Therefore, the bar output is selected by the counter 23 when the offset voltage of the amplifier circuit (-1) is detected by the selector 2. Thus, the same operation as described above can be performed.



The offset voltage value (data) detected and digitized by the counter is held in each of a first register (non-inverse) and a second register (inverse) through a selector 1. Namely, a digital signal (data) corresponding to the offset voltage of the amplifier circuit (+1) is produced and stored in the first register through the selector 1. Thereafter, the counter is cleared. Further, a digital signal (data) corresponding to the offset voltage of the amplifier circuit (-1) is produced and stored in the second register through the selector 1. Thereafter, the counter is cleared.

In the present embodiment, the offset voltages held in the first register (non-inverse) and the second register (inverse) are not used so as to cancel the offset produced between their corresponding first amplifier circuit (+1) and second amplifier circuit (-1). An adder 2 adds together the two offset voltage values (data) held by the two registers. Further, a 1/2 circuit cuts the result of addition in half ($1/2$) so as to calculate the average value of the two offset voltage values (data). The 1/2 circuit may be realized by a simple wiring route in which the simply-added digital output is delivered to a clip circuit 27 in a state of being displaced by one bit, i.e., pointed off by one digit. In this case, the digital output may be sent to the clip circuit 27 in a state of being shifted by one bit with a shift register. The clip circuit 27 is used when it is necessary to restrict the



maximum value of the result of computation, for example. Namely, if the result of computation is less than or equal to the maximum value, then the result of computation (offset cancel data) is transferred to the selector 3 as it is.

An offset control voltage corresponding to the average value with respect to the reference voltage, which is transmitted through the clip circuit 27 and related to each of the two amplifier circuits (+1) and (-1), is inputted to the adder 1 through the selector 3. At this time, the selector 4 selects an original digital signal D0 (data). Namely, each of the average offset voltages is added to the digital signal D0 (data) to be D/A-converted. Thus, the characteristic offset cancel method employed in the present embodiment is intended to provide circuit simplification by allowing the offset voltage corresponding to the difference between the average offset voltages to remain in the offset voltages held by the amplifier circuits (+1) and (-1) judging from the relationship between the input and output of the individual amplifier circuits (+1) and (-1) and transmitting each average offset voltage used as the correction voltage to the difference output circuit through the common adder 1, D/A converter and filter.

Described more specifically, the inconvenience resulting from the existence of the offset between the non-inverse (output) signal and the inverse (output)



signal occurs in the high-frequency unit corresponding to the next-stage circuit. In the present embodiment, the non-inverse (output) signal and the inverse (output) signal at the modem unit are made equal to each other by respectively superimposing the offset voltages or the above average offset voltages thereon. Therefore, the offset voltages are canceled in a manner similar to the noise components in the differential circuit of the high-frequency unit so that no innegligible noise and dc components are produced in the output signal of the differential circuit in the high-frequency unit.

The analog switch 20 is provided with the function of selecting the reference voltage V_{ref} . Namely, the analog switch selects the reference voltage upon the above-described normal operation and serves so as to supply the same reference voltage to the two inputs of the voltage comparator. Thus, the current that flows in the differential circuit constituting the voltage comparator, is made uniform. It is further possible to avoid property degradation that the differential circuit in the voltage comparator is unbalanced due to a change over time.

A selector 5 is provided to input external offset data. Although not restricted in particular, the high-frequency unit will cause inconvenience due to the remaining of offset held by itself even if the modem unit adjusts the offset when the offset occurs in the differential circuit of the high-frequency unit.

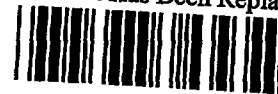


Therefore, the above-described external input function is provided so that the offset control circuit of the modem unit can be used even for the offset control of the high-frequency unit. Namely, a digital signal is formed so as to cancel the offset produced in the high-frequency unit and inputted to the modem unit so that the signal can be processed by the modem unit. Thus, the entire system can be simplified.

A timing generating circuit 29 generates the majority clock signal and the control signals (C1, C2, ... Cn) used for the respective selectors 1 through 5 and supplies them therefrom.

Fig. 3 is a block diagram showing another embodiment of the offset control circuit according to the present invention. In the modem unit 300, unillustrated waveform generating circuits each used as the phase modulator, D/A converters, filters and differential output circuits each used as an output buffer are provided as two pairs of circuits in parallel to obtain signal outputs having a 90° phase difference therebetween, i.e., orthogonal to each other. The offset control circuit is used commonly to the two sets of differential output circuits. In the same drawing, a selector 5 for inputting the above-described offset data and a timing generating circuit 29 are omitted.

Therefore, an analog switch serves so as to select amplifier circuits provided as four in total and the above-described reference voltage. A selector 1 has four



select functions so as to correspond to the provision of four registers in total comprising two sets of non-inverse registers and two sets of inverse registers provided so as to correspond to the above two sets of differential output circuits. Further, the above-described adder 1, a selector 3 and a selector 4 provided at the input of the adder 1, and a clip circuit are respectively provided as two pairs so as to correspond to the two sets of D/A converters. On the other hand, the voltage comparator, majority circuit, counter and adder 2 are time-divisionally commonly used upon offset cancel operations of the four amplifier circuits.

Fig. 4 is a schematic block diagram showing one embodiment of the majority circuit 22 included in the offset control circuit. When the voltage corresponding to the difference between the reference voltage and an input voltage is extremely small, the voltage comparator is affected even by low noise so that the accuracy of decision by the voltage comparator is made worse. Therefore, flip-flops FF1 through FF3 take in or capture an up/down signal 1 outputted from the voltage comparator in synchronism with majority clocks 1 through 3 having times delayed by Δt . Namely, up/down signals 1 produced each time the delay times Δt elapse, are sequentially taken in the flip-flops FF1 through FF3. Signals outputted from the flip-flops FF1 through FF3 are respectively inputted to three inputs AI, BI and CI of a



majority logical circuit LOG so that an up/down signal 2 is produced from an output CO thereof in accordance with a majority decision.

Even if an error up/down signal 1 is formed due to noise, an up/down signal 2 corresponding to each of other two proper up/down signals 1 can be formed owing to the above-described construction. Alternatively, a more correctly-oriented decision result can be obtained even if the reference voltage and the input voltage are equal to each other and the result of decision varies momentarily.

Fig. 5 is a circuit diagram showing one embodiment of the counter control circuit 23-1 included in the counter 23. A count signal is generated in synchronism with a first comparison operation used for offset control. Thus, a first decision result is stored in a flip-flop FF4. When the first decision result is low in level as described above, the flip-flop FF4 is maintained at the low level. Thereafter, an up/down signal 2 is produced from the majority circuit for each comparison operation and counted up or down by the counter. When the signal outputted from the majority circuit changes from a low to a high levels, the low level produced from the flip-flop FF4 and the high level produced from the majority circuit are inputted to the input of an exclusive OR circuit EXOR, so that a high-level count stop signal is produced. This count stop signal is inputted to the counter as a stop signal through an OR circuit together with a carry signal



produced from the counter.

The count operation of the counter is stopped when the decision output firstly produced from the voltage comparator is inverted in response to the count output of the counter. Namely, the above-described flip-flop circuit and exclusive OR circuit can detect two states: one in which the low level is first outputted as the output signal as described above and the output signal is changed to the high level and another in which the high level is first outputted and the output signal is changed to the low level. When the offset voltage falls beyond an offset cancel range, the counter will overflow. The stop signal is generated in response to the carry signal produced from the counter and the maximum or minimum value is outputted as the counted value of the counter.

Fig. 6 shows a potential distribution for describing the offset cancel operation according to the present invention. Assuming that, for example, the offset voltage of the first amplifier circuit (+1) is represented as X and the offset voltage of the second amplifier circuit (-1) is represented as Y, a bar signal is outputted from the counter as the offset voltage Y. Therefore, an average value expressed as $(X + Y)/2 = Z$ is formed. An offset voltage produced from the first amplifier circuit (+1) by adding the average value Z to the offset voltage X is made equal to an offset voltage produced from the second amplifier circuit (-1) by substantially subtracting the



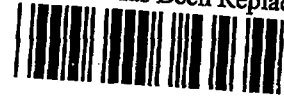
average voltage Z from the offset voltage Y.

Namely, the first amplifier circuit (+1) and the second amplifier circuit (-1) have the synthesized offset voltage referred to above judging from the relationship between the inputs and outputs thereof. However, the two are made equal to each other judging from the relative relationship between the non-inverse output and the inverse output. Therefore, since they are canceled together with noise by the differential circuit in the next-stage high-frequency unit, innegligible noise and dc components are prevented from being produced in the output signal of the differential circuit in the high-frequency unit due to the offset between the amplifier circuits in the modem unit, for forming the non-inverse (output) signal and the inverse (output) signal.

Fig. 7 is a flowchart for describing an offset control operation of the offset control circuit according to the present invention. The offset control operation is performed during a training period prior to the commencement of operation of the modem unit.

When the offset control circuit is started up in Step (1), the selectors 3 through 5 are set in Step (2). Namely, the selector 3 is electrically connected to the selector 2 in response to an offset detecting operation. The selector 4 is set to the DC code output side and the selector 5 is brought to an off state.

In Step (3), either the non-inverse side or the



inverse side is selected. Namely, the selectors 1, 2 and the analog switch are set to either the non-inverse side or the inverse side. In Step (4), a process of making a decision about a voltage comparison is executed. Namely, an up/down signal 2 is produced under the operation of the voltage comparator and the operation of the majority circuit. In Step (5), the counter performs a +1 or -1 count operation in response to the up/down signal 2. In Step (6), the value counted by the counter is set to its corresponding register.

In Step (7), a digital signal obtained by adding the value counted by the counter and the DC code output with the adder 1 is subjected to D/A conversion. In Step (8), the second and later decisions are made. When it is determined in Step (9) that no stop signal is produced (i.e., when the answer is found to be No in Step (9)), the routine procedure is returned to Step (5) referred to above. Thereafter, a loop repetition operation of Steps (5) through (9) referred to above is carried out until the stop signal is generated (the answer is found to be Yes in Step (9)).

If it is determined in Step (9) that the stop signal has been generated (i.e., if the answer is found to be Yes in Step (9)), then the counter is reset in Step (10). It is next determined in Step (11) whether the selection of either the non-inverse side or the inverse side has been completed. If it is determined in Step (11) that the



selection of the inverse side has not yet been completed, for example, then the routine procedure is returned to Step (3), where the inverse side is selected by the analog switch 20 and the selectors 1, 2 and subsequently the same operation as described above is performed.

If it is determined in Step (11) that the selection of both the non-inverse and inverse sides has been completed (i.e., if the answer is found to be Yes in Step (11)), then the values held in a register (non-inverse) and a register (inverse) are added together in Step (12) and the resultant value is subjected to a half ($1/2$) computational process to obtain an average value. In Step (13), the average value produced by the computational process is held by the clip circuit. In Step (14), the selectors 3 and 4 are switched to set the adder 1 so that a data output and offset cancel data are inputted to the adder 1.

When the differential output circuits for performing the offset control exist as two pairs as in the embodiment shown in Fig. 3, it is determined after above Step (14) whether the series of offset cancel operations on both the I and Q signal sides has been completed. After the offset cancel operation of the differential output circuit on the I signal side has been completed, the offset cancel operation of the differential output circuit on the Q signal side may be performed.

Fig. 8 is a timing chart for describing the offset



detecting operation of the offset control circuit according to the present invention. The following operations are successively performed in synchronism with a count signal used as a clock signal. Since the output of the counter is first 0, an output signal designated at numeral 256, which corresponds to a middle voltage, is produced from the adder 1. The D/A converter converts the output signal into an analog voltage. Thus, a non-inverse (output) signal is outputted from the first amplifier circuit (+1). When the non-inverse (output) signal is lower than the reference voltage, an up/down signal 2 is rendered high in level. Thereafter, the counter counts +1 as the counter output in synchronism with the count signal. The counter output is transferred to the register (non-inverse) and the output of the adder 1 is increased to 257 so that the non-inverse (output) signal is rendered high by its increase. The non-inverse (output) signal is increased one by one in turn according to the above-described count operation of the counter. When it exceeds the reference voltage, the up/down signal 2 changes from a high to a low levels. In response to this change, a stop signal is generated to stop the operation of the counter. As a result, the counter is cleared and hence restored to 0.

The analog switch and the selector 2 are switched to perform the offset detecting operation on the inverse side. Since the output of the counter is first 0 in the same



manner as described above, an output signal designated at numeral 256, which corresponds to a middle voltage is produced from the adder 1. The D/A converter converts it into an analog voltage so that an inverse (output) signal is produced from the second amplifier circuit (-1). When the inverse signal is lower than the reference voltage, the up/down signal 2 is rendered high in level.

Afterwards, the counter counts +1 as a counter output in synchronism with the count signal. However, since the bar ~~output~~ output is selected by the selector 2 as the counter output, ~~=~~ the counter substantially performs a -1 count operation so as to reduce its counted value to -1. -1 is transferred to the corresponding register. The output of the adder 1 is reduced to 255 so that the inverse output is increased correspondingly. The inverse output is sequentially raised in level in response to the count operation of the counter. When the inverse output exceeds the reference voltage, the up/down signal 2 changes from the high level to the low level. In response to its change, the stop signal is produced to stop the operation of the counter, so that the counter is cleared and hence restored to 0.

In addition to the transfer of the data to each register for each uniform count operation, the data transfer may be performed only once by controlling the selector 1 upon formation of the stop signal since it is useless to store the counted value in the corresponding register in the course of the above-described operation.



The above-described control on the counter can adopt various forms. One method is that the count data is sequentially counted up (+1) or down (-1) from zero in accordance with the up/down signal 2 as described above.

In the control method referred to above, the voltage comparator forms or produces a high-level or low-level up/down signal 1 even when the offset voltage is close to zero unlimitedly as described above. As a result, the output of the voltage comparator is no longer inverted under the subsequent operation as described above and the offset-voltage detecting operation is performed until the counter is carried over. Therefore, there is a possibility that the counter is activated until the maximum value of the counter is reached, thereby misdetermining that the maximum offset voltage exists.

A second method is that the counter is initially set to the minimum or maximum value and when the offset voltage falls within the offset cancel range, the up/down signal 2 is assuredly changed from one level to another level.

The second method needs to activate the counter over the range from the minimum value to the maximum value at worst and to spend a relatively long time for the offset detection.

According to a third method, the counter is set to zero and count data is set to the maximum or minimum value in response to an up/down signal at the time of the



setting of the counter to zero, followed by starting of the offset detecting operation. Thus, when the count data falls between the maximum or minimum value and zero, the offset voltage can be detected so as to deactivate the counter.

Fig. 9 is a schematic block diagram showing one embodiment of the high-frequency unit. Of the two sets of differential output signals formed by the modem unit including the offset control circuit, the non-inverse signal (I) and the inverse output (IB) both defined as the first pair are inputted to a differential circuit AMP1 to thereby cancel the above-described noise and offset, whereby a doubled I signal is produced from the differential circuit AMP1.

The non-inverse signal (Q) and the inverse output (QB) both defined as the second pair are inputted to a differential circuit AMP2 to thereby cancel the above-described noise and offset, whereby a doubled Q signal is produced from the differential circuit AMP2. The Q signal is phase-shifted by 90° by a phase circuit 900. An addition circuit 901 adds the phase-shifted Q signal and the I signal together. Further, a multiplication circuit 903 superimposes the result of addition on a carrier produced by a synthesizer 902 and outputs it as a transmitting radio wave.

The differential circuits AMP1 and AMP2 are used in the high-frequency unit as described above. Further, when



the offset is included in each differential circuit, dc components corresponding to offset voltages remain in the output signals I and Q. If the offset voltages of the differential circuits AMP1 and AMP2 in the high-frequency unit are detected and the detected voltages are converted into digital form and inputted as the external offset data for the modem unit, which is shown in Fig. 2, then the offset voltage produced in the high-frequency unit can be also canceled by using the offset control circuit provided within the modem unit. In Fig. 1, a route indicated by the broken line, which extends from the high-frequency unit 400 to the input/output circuit 308 of the modem unit 300, shows the above-described external offset data.

Operations and effects obtained from the above-described embodiments are as follows:

(1) A D/A conversion output circuit having a D/A converter, a first amplifier circuit for producing a non-inverse output signal being in phase with an output signal produced from the D/A converter in response to the output signal thereof and a second amplifier circuit for producing an inverse output signal opposite in phase to the output signal produced from the D/A converter in response to the output signal thereof, can bring about an advantageous effect in that offset voltages of the first and second amplifier circuits, each of which corresponds to an analog middle voltage, are respectively detected and the average value thereof processed in digital form is



added to an input digital signal of the D/A converter, whereby offset can be canceled on the next-stage differential circuit side receiving the non-inverse output signal and the inverse output signal therein.

(2) In the paragraph (1) referred to above, another advantageous effect can be brought about in that since an offset control circuit is not intended to cancel the offset with respect to each of the first and second amplifier circuits but can be used commonly to the two amplifier circuits, the D/A conversion output circuit can be simplified.

(3) A further advantageous effect can be brought about in that since the offset control circuit can be shared between both an offset detection and offset control by providing selectors at the inputs of the adder, supplying only a digital signal corresponding to a middle voltage during the first period, supplying a signal outputted from the counter as a signal to be added, during a second period and supplying a signal outputted from a clip circuit and the input digital signal during a D/A conversion operation, the efficiency of usage of the offset control circuit can be enhanced, so that the D/A conversion output circuit can be substantially simplified.

(4) A still further advantageous effect can be brought about in that a high-accuracy voltage comparison output can be obtained by providing at the output of the voltage comparator, a flip-flop circuit for time-



sequentially successively capturing large and small comparison output signals in synchronism with a clock signal (pulse) and a majority circuit for receiving a signal outputted from the flip-flop circuit and by using a signal outputted from the majority circuit as the above large or small comparison output.

(5) A still further advantageous effect can be brought about in that an offset voltage of a differential circuit in the next-stage high-frequency unit can be canceled by allowing external offset data to be selectively inputted to the adder.

(6) A still further advantageous effect can be obtained in that the D/A conversion output circuit can be simplified by providing the D/A converter and the first and second amplifier circuits as two sets so as to correspond to I and Q signals and sharing the offset control circuit between the two sets of D/A converters and first and second amplifier circuits.

(7) A still further advantageous effect can be brought about in that the analog switch is able to keep the property of the voltage comparator satisfactory with the change in time by supplying a reference voltage when the offset control circuit is in a deactivated state, to thereby make both voltages inputted to the voltage comparator equal to each other.

The invention made by the present inventors has been specifically described based on the embodiments as



mentioned above. However, the invention of the present application is not necessarily limited to the aforementioned embodiments. It is needless to say that various changes and modifications can be made without departing from the spirit or scope of the invention as set forth herein. For instance, the up/down signal 2 to be outputted from the majority circuit may be inverted upon offset detection on the inverse side so as to be inputted to the counter circuit. In this case, the selector 2 can be omitted. The present invention can be widely used as an offset control circuit for a D/A conversion output circuit having an output buffer for producing a non-inverse output signal and an inverse output signal corresponding to D/A-converted analog signals.

Advantageous effects obtained by typical ones of the inventions disclosed in the present application will be described in brief as follows: In a D/A conversion output circuit having a D/A converter, a first amplifier circuit for producing a non-inverse output signal being in phase with an output signal produced from the D/A converter in response to the output signal thereof, and a second amplifier circuit for producing an inverse output signal opposite in phase to the output signal produced from the D/A converter in response to the output signal thereof, the offset can be canceled on the next-stage differential circuit side receiving the non-inverse output and the inverse output owing to a simple configuration that offset



voltages of the first and second amplifier circuits, each of which corresponds to an analog middle voltage, are respectively detected and the average value thereof processed in digital form is added to an input digital signal of the D/A converter.



What is claimed is:

1. A digital/analog conversion output circuit comprising:

a digital/analog converter;

a first amplifier circuit for producing a non-inverse output signal being in phase with a signal outputted from said digital/analog converter, in response to the output signal thereof;

a second amplifier circuit for producing an inverse output signal opposite in phase to the signal outputted from said digital/analog converter in response to said output signal thereof; and

an offset control circuit for detecting digitized offset voltages of said first and second amplifier circuits, each corresponding to an analog middle voltage, determining an average value of the two offset voltages and adding the average value to a digital signal to be inputted to said digital/analog converter.

2. A digital/analog conversion output circuit comprising:

a digital/analog converter;

a low-pass filter for eliminating high-frequency components included in a signal outputted from said digital/analog converter;

a first amplifier circuit for producing a non-inverse





output signal being in phase with a signal outputted from said low-pass filter, in response to the output signal thereof;

a second amplifier circuit for producing an inverse output signal opposite in phase to the output signal of said digital/analog converter in response to the output signal thereof; and

an offset control circuit including,

a first adder for producing a digital signal to be supplied to said digital/analog converter;

an analog switch for selecting signals outputted from said first and second amplifier circuits;

a voltage comparator for making a magnitude comparison between an output voltage value supplied through said analog switch and a reference voltage value corresponding to a middle voltage value of the input signal;

a counter for performing an up or down count operation in response to the large or small comparison output obtained from said voltage comparator;

first and second registers for respectively holding an output counted by said counter;

a second adder for adding together signals outputted from said first and second registers; and

a clip circuit for holding a signal corresponding to the half of a signal outputted from said second adder;





whereby during a first period prior to a digital/analog conversion operation of said digital/analog conversion output circuit, a digital signal corresponding to the middle voltage is inputted to a first input of said first adder so as to output an output signal corresponding to the digital signal, and said analog switch allows said counter to perform the up or down count operation in response to the large or small comparison output obtained by making a comparison between the signal outputted from said first amplifier circuit and the reference voltage with said voltage comparator,

during a second period, the signal outputted from said counter is supplied to a second input of said first adder so as to output a signal obtained by adding together the signals inputted to the first and second inputs, and said analog switch allows said counter to repeatedly perform the up or down count operation in response to the large or small comparison output obtained by making a comparison between the signal outputted from said first amplifier circuit and the reference voltage with said voltage comparator,

during a third period, said operation is stopped when the large or small comparison output produced from said voltage comparator is inverted and a value counted by said counter at this time is transferred to said first register,

during a fourth period, the digital signal corresponding to the middle voltage is inputted to the





first input of the first adder so as to produce an output signal corresponding to the digital signal, and said analog switch allows said counter to perform the up or down count operation in response to the large or small comparison output obtained by comparing the output signal of said second amplifier circuit and the reference voltage with said voltage comparator,

during a fifth period, the output signal of said counter is supplied to the second input of said first adder so as to output a signal obtained by adding together the signals inputted to the first and second inputs, and said analog switch allows said counter to repeatedly perform the up or down count operation in response to the large or small comparison output obtained by making a comparison between the signal outputted from said first amplifier circuit and the reference voltage with said voltage comparator,

during a sixth period, said operation is stopped when the large or small comparison output produced from said voltage comparator is inverted and a value counted by said counter at this time is transferred to said second register, and

during a seventh period, the output signals of said first and second registers are added together by said second adder and a signal corresponding to the half of the added output is held by the clip circuit and added to the digital signal by said first adder.





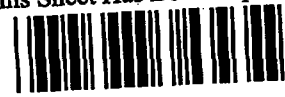
3. A digital/analog conversion output circuit according to claim 2, wherein selectors are provided at the inputs of said first adder so as to supply only the digital signal corresponding to the middle voltage during the first period, supply the output signal of said counter as a signal to be added during the second period and supply the signal outputted from the clip circuit and the digital signal during the digital/analog conversion operation.

4. A digital/analog conversion output circuit according to claim 1, 2 or 3, wherein a flip-flop circuit for time-sequentially successively capturing large and small comparison output signals in synchronism with a clock signal and a majority circuit for receiving a signal outputted from the flip-flop circuit are provided at the output of said voltage comparator and a signal outputted from the majority circuit is used as the large or small comparison output.

5. A digital/analog conversion output circuit according to claim 1, 2, 3 or 4, wherein said first adder is provided with a selector for allowing external offset data to be selectively inputted thereto.

6. A digital/analog conversion output circuit





according to claim 2, wherein said digital/analog converter and said first and second amplifier circuits are respectively provided in two pairs, which share the use of said analog switch, said voltage comparator, said counter and said second adder, and said first adder, said first and second registers and said clip circuit are respectively provided in two pairs.

7. A digital/analog conversion output circuit according to claim 2, wherein said analog switch is provided with connecting switch routes for supplying a reference voltage when said offset control circuit is in a deactivated state and equalizing two input voltages supplied to said voltage comparator.

8. A digital/analog conversion output circuit according to claim 2, 3, 4 and 5, wherein said analog switch has connecting switch routes for supplying a reference voltage when said offset control circuit is in a deactivated state and equalizing two input voltages supplied to said voltage comparator.

9. A portable communication terminal comprising:
an antenna for transmitting first digital data to be transmitted;

a high-frequency unit for amplifying and modulating the first digital data; and





a modem unit having a converting circuit for converting the first digital data into first analog data and supplying it to said high-frequency unit, said converting circuit including,

a digital/analog converter;

a low-pass filter for eliminating high-frequency components included in a signal outputted from said digital/analog converter;

a first amplifier circuit for producing a non-inverse output signal being in phase with a signal outputted from said low-pass filter, in response to the output signal thereof;

a second amplifier circuit for producing an inverse output signal opposite in phase to the output signal of said digital/analog converter in response to the output signal thereof; and

an offset control circuit for controlling an offset produced between the non-inverse output signal and the inverse output signal, said offset control circuit further including,

a first adder for producing a digital signal to be supplied to said digital/analog converter;

an analog switch for selecting signals outputted from said first and second amplifier circuits;

a voltage comparator for making a magnitude comparison between an output voltage value supplied through said analog switch and a reference voltage value





corresponding to a middle voltage value of the input signal;

a counter for performing an up or down count operation in response to the large or small comparison output obtained from said voltage comparator;

first and second registers for respectively holding an output counted by said counter;

a second adder for adding together signals outputted from said first and second registers; and

a clip circuit for holding a signal corresponding to the half of a signal outputted from said second adder.

10. A portable communication terminal according to claim 9, wherein said modem unit includes a waveform generating circuit for phase-modulating the first digital data.

