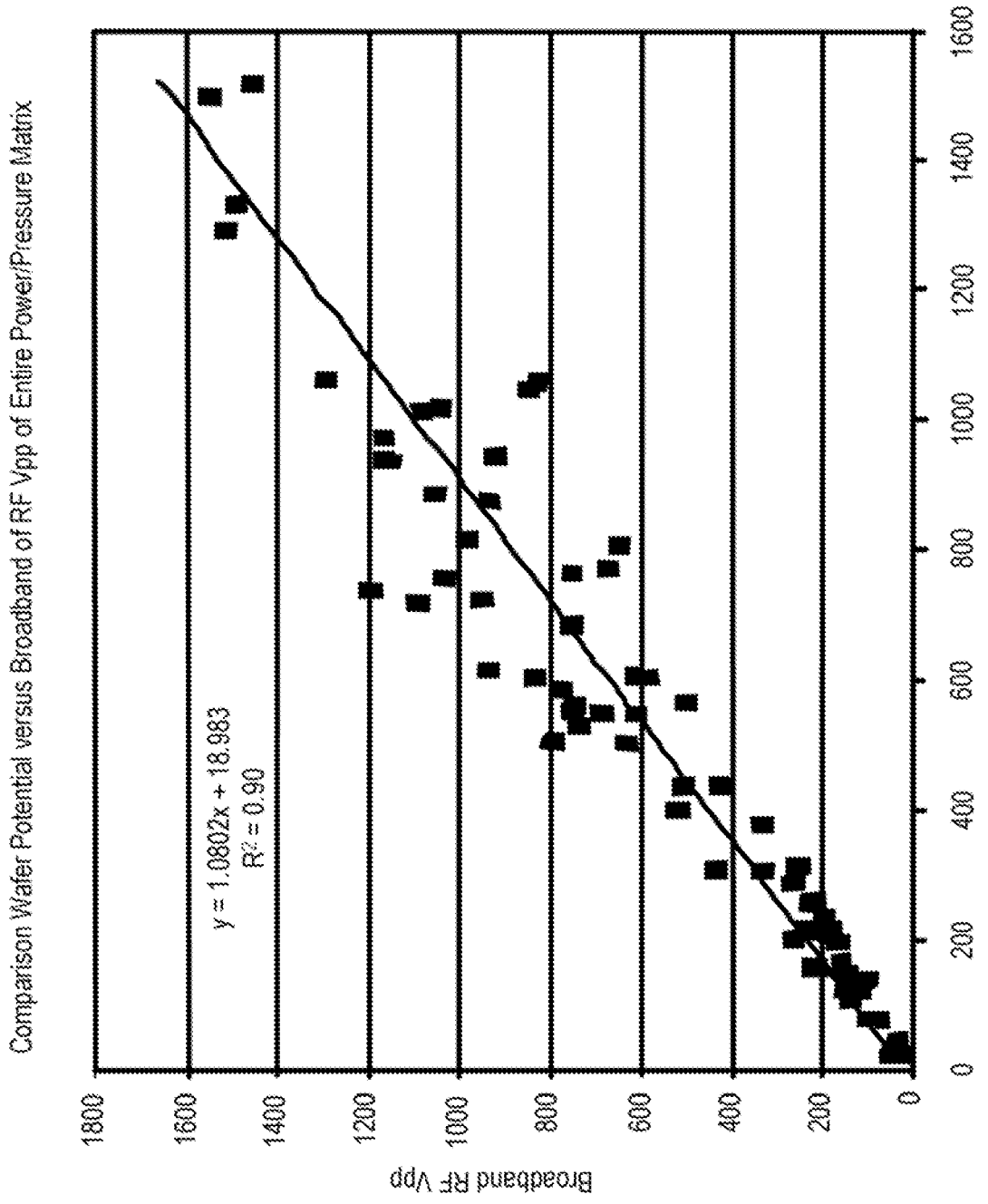

Comparison Wafer Potential versus Broadband of RF Vpp of Entire Power/Pressure Matrix
y = 1.0802x + 18.983
R² = 0.90
Broadband RF Vpp
Wafer Potential
0
200
400
600
800
1000
1200
1400
1600
1800

FIGURE 1

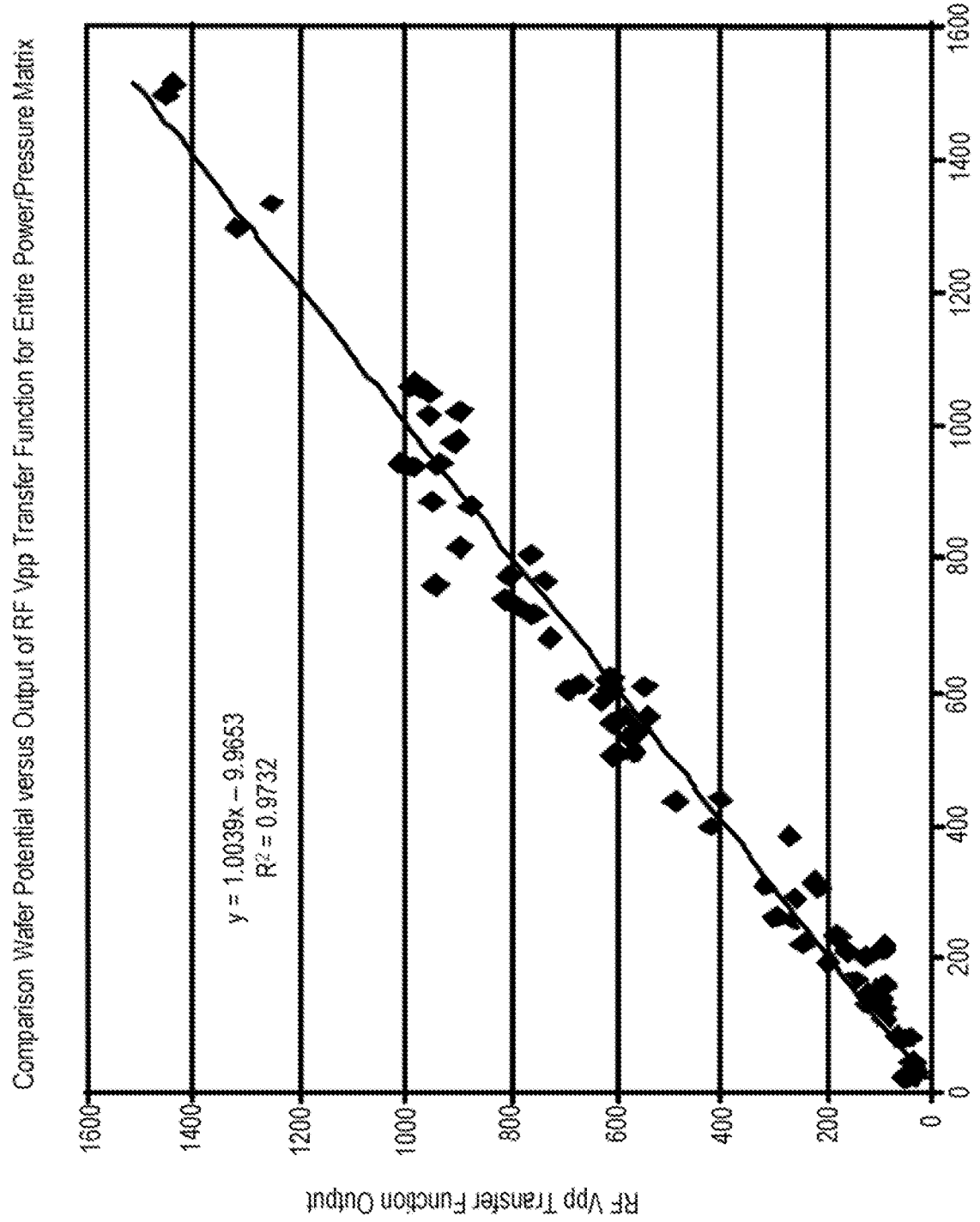

Comparison Wafer Potential versus Output of RF Vpp Transfer Function for Entire Power/Pressure Matrix
y = 1.0039x – 9.9653
R² = 0.9732
RF Vpp Transfer Function Output
Wafer Potential
0
200
400
600
800
1000
1200
1400
1600

FIGURE 2

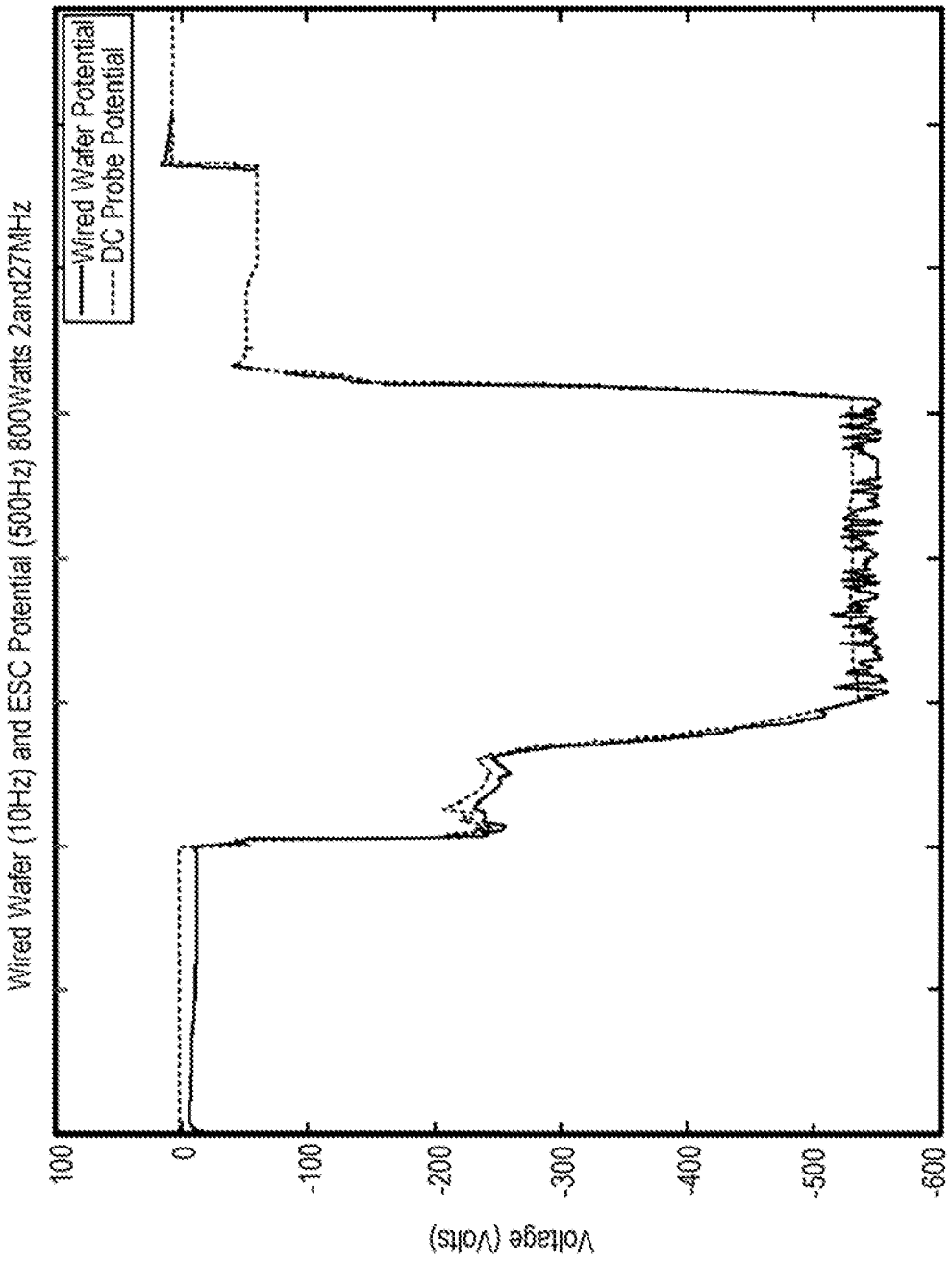

Wired Wafer (10Hz) and ESC Potential (500Hz) 800Watts 2and27MHz
Wired Wafer Potential
DC Probe Potential
Voltage (Volts)
100
0
-100
-200
-300
-400
-500
-600
0
10
20
30
40
50
60
70
Time (seconds)

FIGURE 3

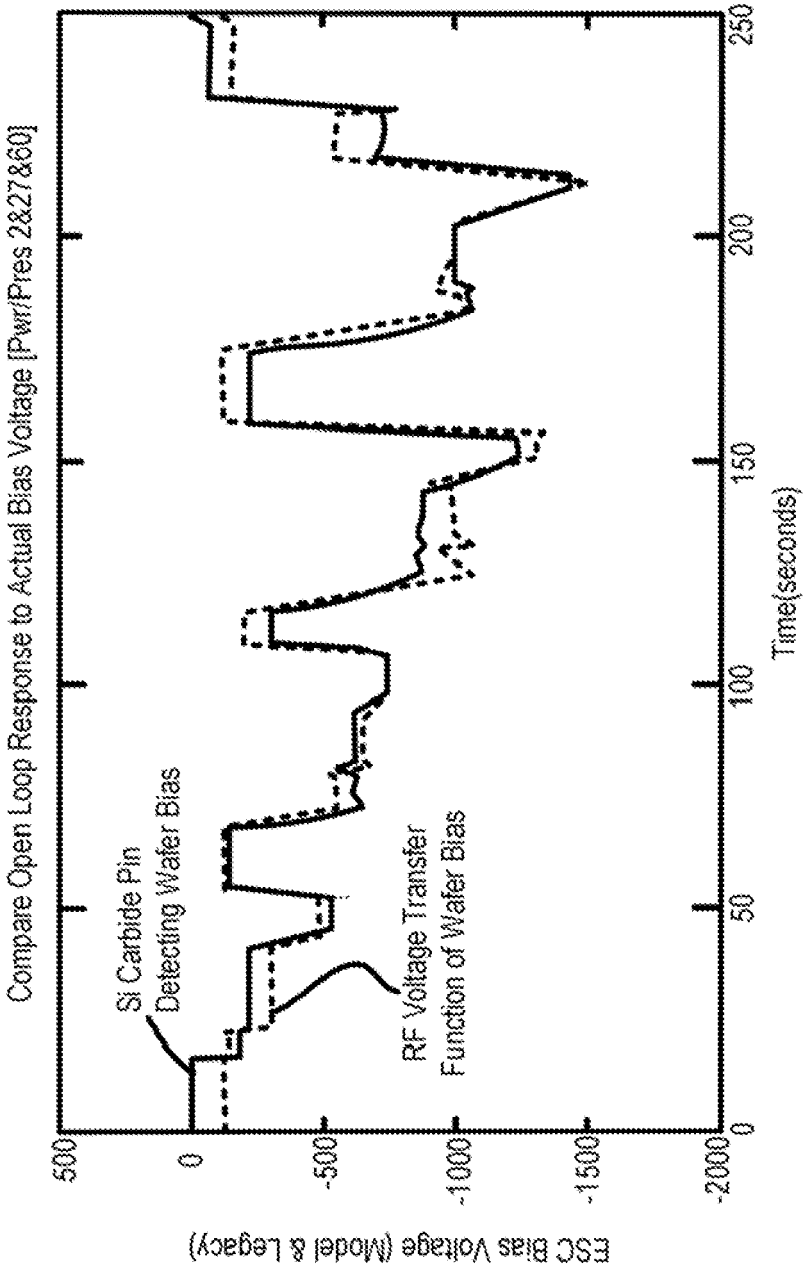

Compare Open Loop Response to Actual Bias Voltage [Pwr/Pres 2&27&60]
Si Carbide Pin
Detecting Wafer Bias
RF Voltage Transfer
Function of Wafer Bias
ESC Bias Voltage (Model & Legacy)
Time(seconds)
500
0
-500
-1000
-1500
-2000
0
50
100
150
200
250

FIGURE 4

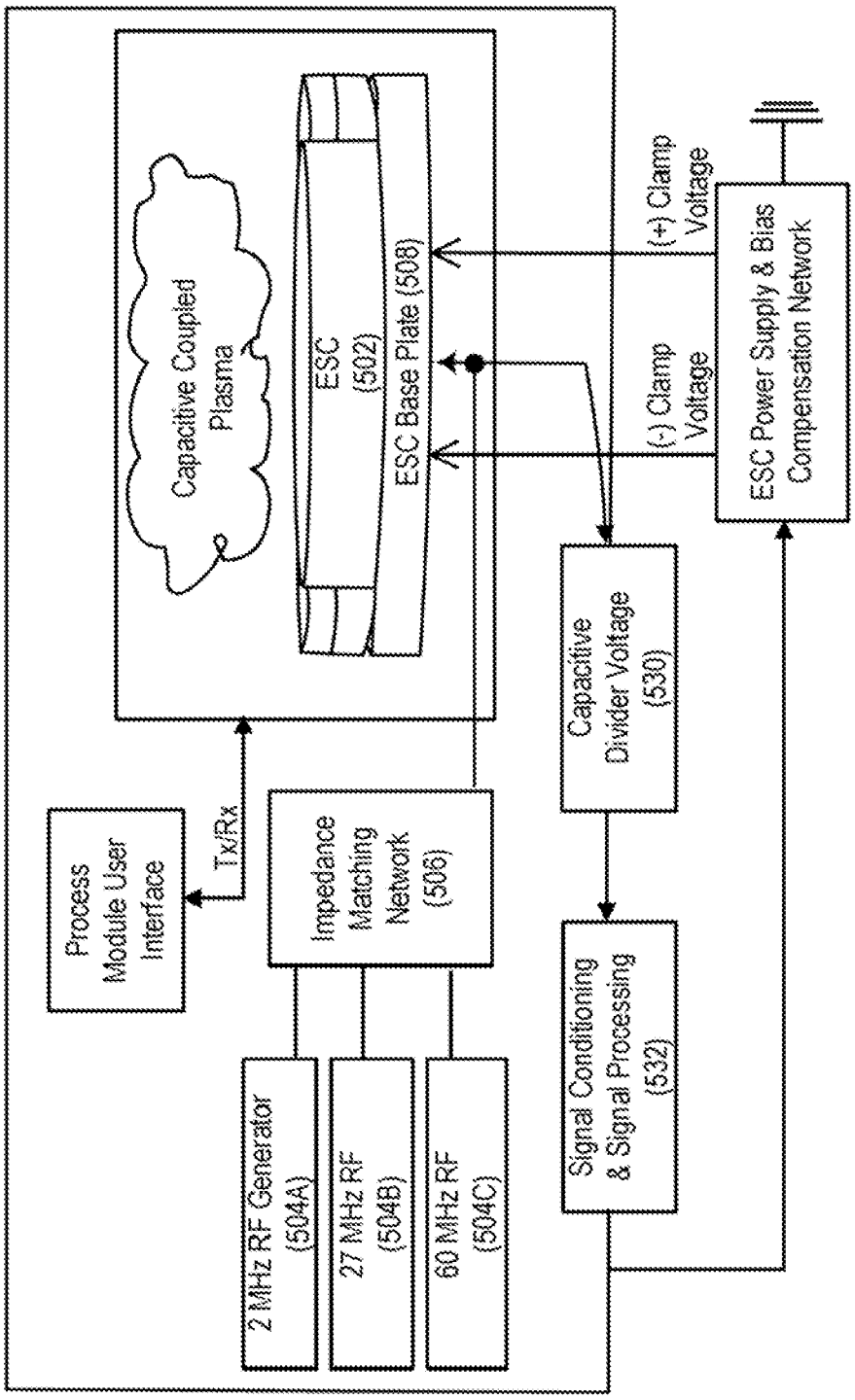

Capacitive Coupled Plasma
ESC (502)
ESC Base Plate (508)
(+) Clamp Voltage
(-) Clamp Voltage
ESC Power Supply & Bias Compensation Network
Capacitive Divider Voltage (530)
Process Module User Interface
Tx/Rx
Impedance Matching Network (506)
2 MHz RF Generator (504A)
27 MHz RF (504B)
60 MHz RF (504C)
Signal Conditioning & Signal Processing (532)

FIGURE 5A

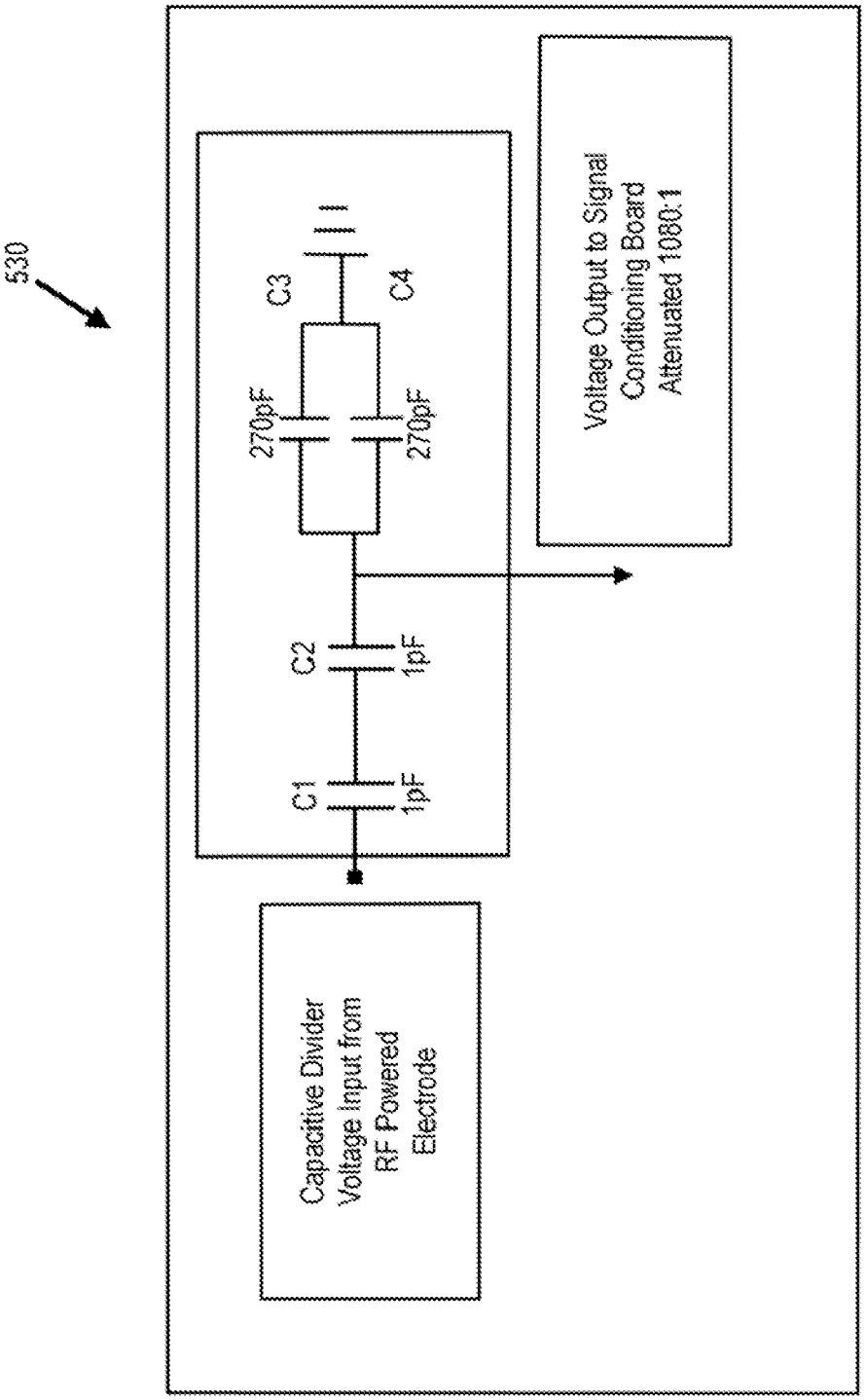

530
Capacitive Divider
Voltage Input from
RF Powered
Electrode
C1
1pF
C2
1pF
C3
270pF
C4
270pF
Voltage Output to Signal
Conditioning Board
Attenuated 1080:1

FIGURE 5B

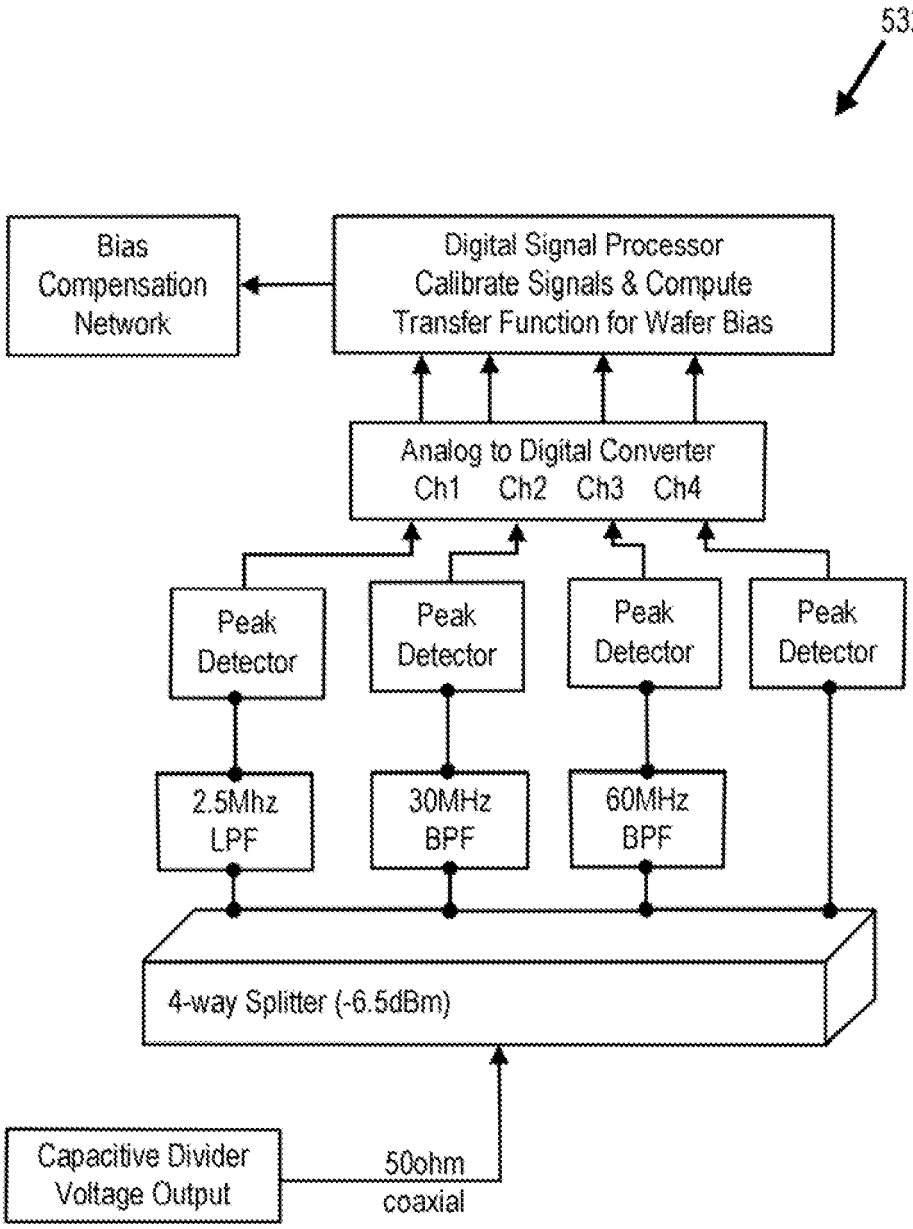

532
Bias Compensation Network
Digital Signal Processor Calibrate Signals & Compute Transfer Function for Wafer Bias
Analog to Digital Converter Ch1 Ch2 Ch3 Ch4
Peak Detector
Peak Detector
Peak Detector
Peak Detector
2.5Mhz LPF
30MHz BPF
60MHz BPF
4-way Splitter (-6.5dBm)
Capacitive Divider Voltage Output
50ohm coaxial

FIGURE 5C

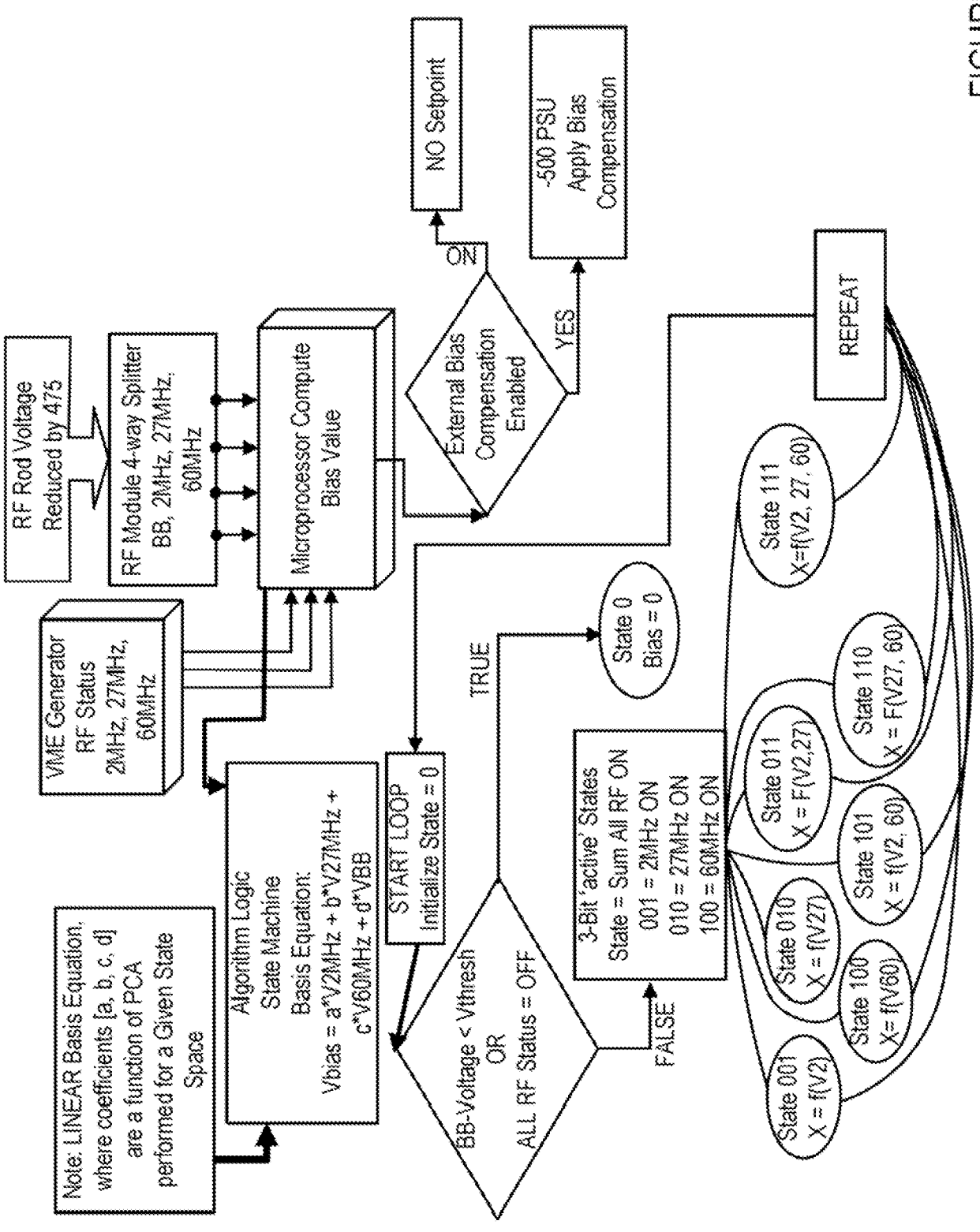

RF Rod Voltage Reduced by 475
RF Module 4-way Splitter BB, 2MHz, 27MHz, 60MHz
Microprocessor Compute Bias Value
External Bias Compensation Enabled
NO Setpoint
-500 PSU Apply Bias Compensation
YES
NO
VME Generator RF Status 2MHz, 27MHz, 60MHz
Note: LINEAR Basis Equation, where coefficients [a, b, c, d] are a function of PCA performed for a Given State Space
Algorithm Logic State Machine Basis Equation: Vbias = a*V2MHz + b*V27MHz + c*V60MHz + d*VBB
START LOOP Initialize State = 0
BB-Voltage < Vthresh OR ALL RF Status = OFF
TRUE
FALSE
State 0 Bias = 0
3-Bit 'active' States State = Sum All RF ON 001 = 2MHz ON 010 = 27MHz ON 100 = 60MHz ON
State 001 X = f(V2)
State 010 X = f(V27)
State 100 X= f(V60)
State 101 X = f(V2, 60)
State 011 X = F(V2,27)
State 110 X = F(V27, 60)
State 111 X=f(V2, 27, 60)
REPEAT

FIGURE 6

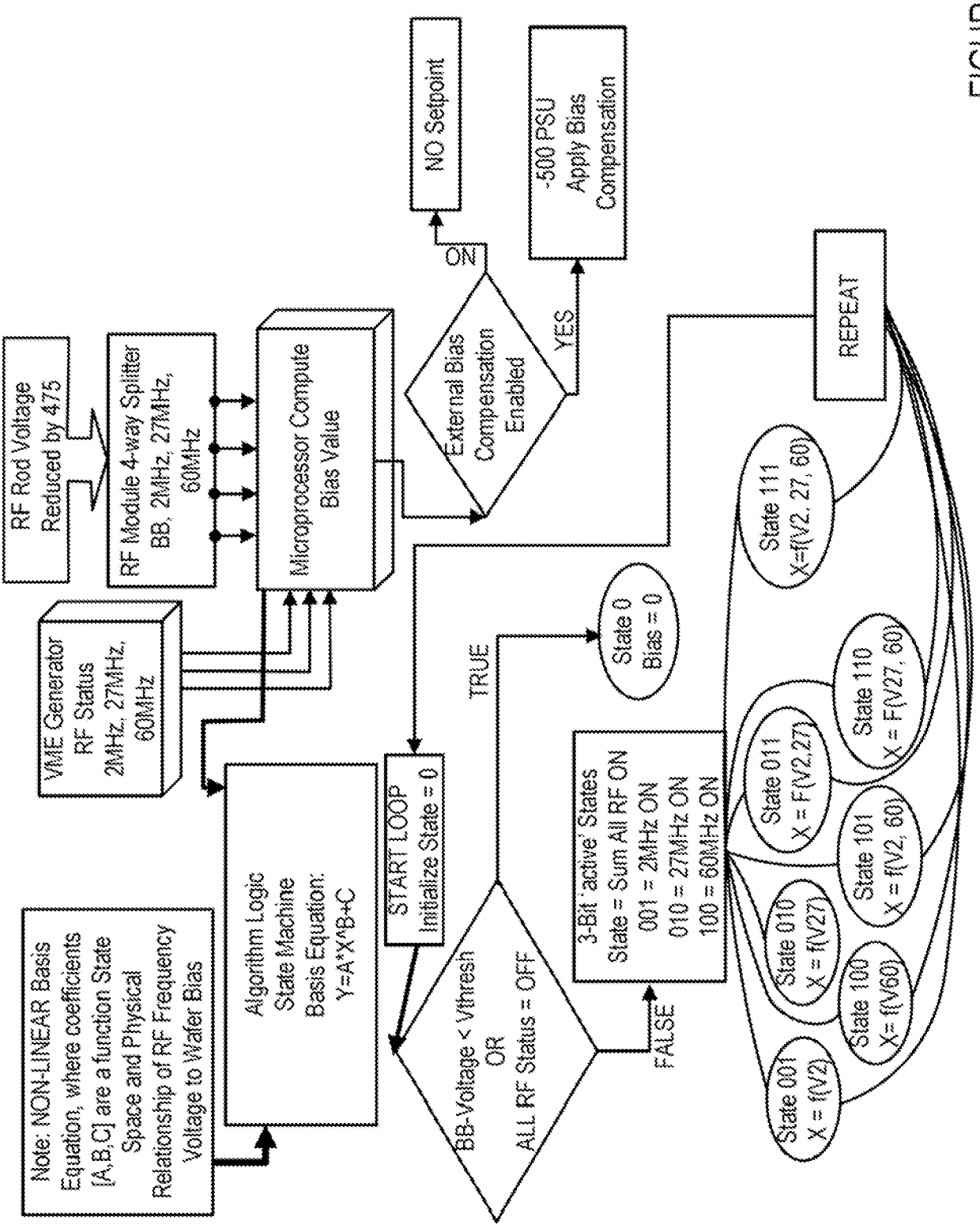

RF Rod Voltage Reduced by 475
RF Module 4-way Splitter BB, 2MHz, 27MHz, 60MHz
Microprocessor Compute Bias Value
NO Setpoint
-500 PSU Apply Bias Compensation
ON
YES
External Bias Compensation Enabled
VME Generator RF Status 2MHz, 27MHz, 60MHz
Algorithm Logic State Machine Basis Equation: Y=A*X^B+C
START LOOP Initialize State = 0
TRUE
State 0 Bias = 0
REPEAT
Note: NON-LINEAR Basis Equation, where coefficients [A,B,C] are a function State Space and Physical Relationship of RF Frequency Voltage to Wafer Bias
BB-Voltage < Vthresh OR ALL RF Status = OFF
FALSE
3-Bit 'active' States State = Sum All RF ON 001 = 2MHz ON 010 = 27MHz ON 100 = 60MHz ON
State 111 X=f(V2, 27, 60)
State 011 X = F(V2,27)
State 110 X = F(V27, 60)
State 010 X = f(V27)
State 101 X = f(V2, 60)
State 100 X= f(V60)
State 001 X = f(V2)

FIGURE 7

How are the 2 methods Different?

- Initial Method Utilizes MVA [multivariate analysis] to create a LINEAR Transfer Function
  - PLS (partial least squares) implemented for each state space to create linear transfer function [RF Voltage to Wafer Bias]
- Current Method Utilizes Non-Linear Transfer Function [power equation]
  - Power Equation used based on existing Physical Relationship of RF Power to RF Voltage
    - Voltage = sqrt(Power / R)
      - This can be rewritten to V = a * (Power/|Z|) ^ b + c
        - In Theory, a = 1, b = .5, and c = 0
  - Impedance of the Plasma is a Function of RF Power Delivered *as well as* Process Parameter [Chemistry, Pressure, Flow, Chamber Coupling (Capacitive/Inductive)]
  - First Order Approximation, V_wafer_dc = V_rf
- For a given Frequency, Explicit Power Equation Can be Used to Relate RF Voltage to Wafer DC Voltage
  - V_wafer_dc = a * V_rf ^ b + c
    - Coefficients a, b, c are optimized to cover entire operating range of Plasma impedance for a given Frequency

FIGURE 8

Further Details

- 7 state spaces exist
  - For single frequency, single equation exists (V_wafer_dc = a * Vpp ^ b + c)
    - Coefficient {a} is bounded by [.3 3]
    - Coefficient {b} is bounded by [.5 and 1] (can never be greater than one)
    - Coefficient {c} is typically 0, (more or less compensate for measurement inaccuracy)
  - For multi frequency state
    - Each Frequency's contribution is computed based upon Single Frequency Transfer Function
    - Individual Frequency's contributions are Summed together
    - Final Result, V_wafer_dc = a * V_summation ^ b + c
      - Coefficients {a, b, c} have same bounds

- WHY Does this work?
  - Revisiting V = sqrt(Power / |Z|) , and first order approximation V_wafer_dc = V_rf
  - Coefficient {a} is a function of Plasma Impedance
  - Coefficient {b} is a function of RF Voltage Peak Detection Method
  - Coefficient {c} is a function of calibration

FIGURE 9

Further Details

- In theory, you could simply have one power equation
  - V_wafer_dc = a * (Sum(RF_Pwr_2MHz/|Z2MHz| + RF_Pwr_27MHz/|Z27Mhz| + RF_Pwr_60MHz/|Z60MHz|)) ^ b + c
  - Coefficients {a,b,c} where optimized to account for accuracy/precision of Delivered Power and Plasma Impedance Measurements

FIGURE 10

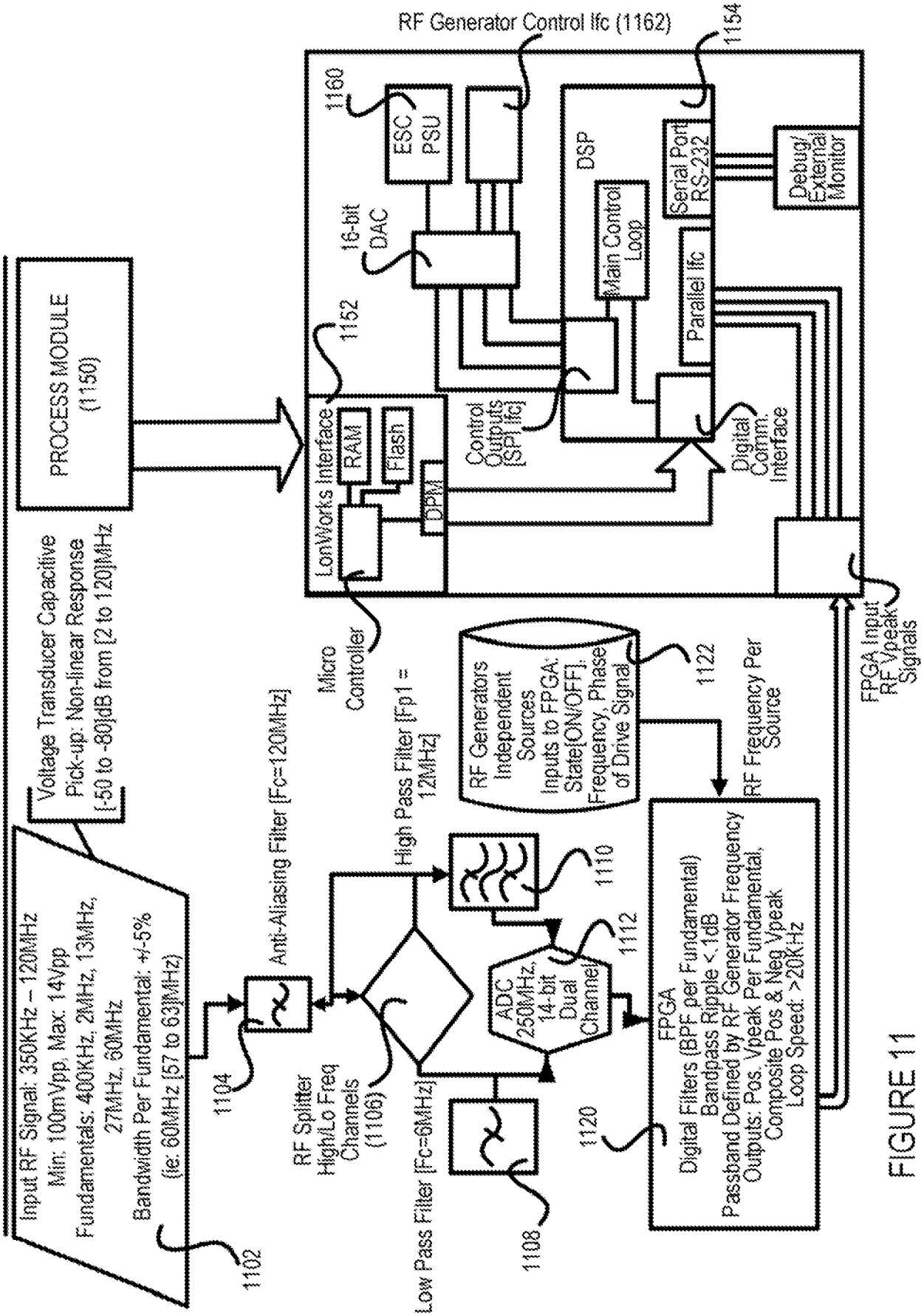

RF Generator Control Ifc (1162)
1154
1160
ESC PSU
16-bit DAC
DSP
Main Control Loop
Serial Port RS-232
Debug/ External Monitor
Parallel Ifc
1152
LonWorks Interface
RAM
Flash
DPM
Control Outputs [SPI Ifc]
Digital Comm. Interface
PROCESS MODULE (1150)
Micro Controller
FPGA Input RF Vpeak Signals
Voltage Transducer Capacitive Pick-up: Non-linear Response [-50 to -80]dB from [2 to 120]MHz
Input RF Signal: 350KHz – 120MHz
Min: 100mVpp, Max: 14Vpp
Fundamentals: 400KHz, 2MHz, 13MHz, 27MHz, 60MHz
Bandwidth Per Fundamental: +/-5%
(ie: 60MHz [57 to 63]MHz)
1102
1104
Anti-Aliasing Filter [Fc=120MHz]
RF Splitter High/Lo Freq Channels (1106)
High Pass Filter [Fp1 = 12MHz]
Low Pass Filter [Fc=6MHz]
1108
1110
ADC 250MHz, 14-bit Dual Channel
1112
RF Generators Independent Sources
Inputs to FPGA: State[ON/OFF], Frequency, Phase of Drive Signal
1122
RF Frequency Per Source
1120
FPGA
Digital Filters (BPF per Fundamental)
Bandpass Ripple <.1dB
Passband Defined by RF Generator Frequency
Outputs: Pos. Vpeak Per Fundamental, Composite Pos & Neg Vpeak
Loop Speed: >20KHz

FIGURE 11