

A PROCESS HAVING HIGH TOLERANCE TO BURIED CONTACT MASK MISALIGNMENT
BY USING A PSG SPACER
ABSTRACT

A new method of forming improved buried contact junctions is described. A layer of polysilicon overlying gate silicon oxide is provided over the surface of a semiconductor substrate and etched away to provide an opening to the substrate where a planned buried contact junction will be formed. A second doped polysilicon layer and a tungsten silicide layer are deposited and patterned to provide gate electrodes and a contact overlying the planned buried contact junction and providing an opening to the substrate where a planned source/drain region will be formed adjoining the planned buried contact junction and wherein a portion of the polysilicon layer not at the polysilicon contact remains as residue. The residue is etched away whereby a trench is etched into the substrate at the junction of the planned source/drain region and the planned buried contact junction. A doped glassaceous layer is deposited overlying the patterned tungsten silicide/polysilicon layer and within the trench, then isotropically etched away until it remains only partially filling the trench. The substrate is oxidized to drive-in dopant from the doped glassaceous layer within the trench into the surrounding substrate. Ions are implanted to form the planned source/drain region. Dopant is outdiffused from the second polysilicon layer to form the planned buried contact junction wherein the dopant surrounding the trench provides a conduction channel between the source/drain region and the adjoining buried contact junction.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)