ABSTRACT

A non-volatile memory device includes a first semiconductor layer including a first cell region in which a first memory cell array is disposed, a second cell region in which a second memory cell array is disposed, wherein the first memory cell array and the second memory cell array each include a plurality of word lines, a plurality of memory cells, and a plurality of bit lines, and a second semiconductor layer including a page buffer circuit region in which a page buffer circuit connected to the first memory cell array and the second memory cell array is disposed, wherein the page buffer circuit region overlaps a boundary region between the first cell region and the second cell region when viewed from the vertical direction.

FIG. 1