CLAIMS

1. A differential inverter amplifier assembly, comprising:

a p-type channel metal oxide semiconductor current source;

a p-type channel metal oxide semiconductor mirror coupled with the p-type channel metal oxide semiconductor current source and configured to provide a bias current;

an n-type channel metal oxide semiconductor current source;

a feedback amplifier configured to adjust the n-type channel metal oxide semiconductor current source to set a common mode voltage; and

a differential inverter amplifier electrically coupled between the p-type channel metal oxide semiconductor current source and the n-type channel metal oxide semiconductor current source, the differential inverter amplifier including a plurality of load resistors and a plurality of diode-connected metal oxide semiconductor clamps.

2. The differential inverter amplifier assembly of claim 1 wherein the plurality of load resistors is configured to enable optimization of gain and bandwidth.

3. The differential inverter amplifier assembly of claim 1 plurality of diode-connected metal oxide semiconductor clamps is configured to limit output swing and minimize common mode disturbances independent of the plurality of load resistors.

4. The differential inverter amplifier assembly of claim 1 further comprising a differential resistive load configured to improve bandwidth and minimize common mode feedback control.

5. The differential inverter amplifier assembly of claim 4 wherein the p-type channel metal oxide semiconductor current source has a voltage vdd.

6. The differential inverter amplifier assembly of claim 5 wherein the common mode voltage is equal to vdd/2.

7. A method for implementing a differential inverter amplifier topology, comprising:

receiving a first current from a p-type channel metal oxide semiconductor current source at a differential inverter amplifier electrically coupled between an input and an output;

receiving a second current from an n-type channel metal oxide semiconductor current source at the differential inverter amplifier;

generating a common mode voltage using the n-type channel metal oxide semiconductor current source and a feedback amplifier coupled with the n-type channel metal oxide semiconductor current source;

limiting output swing by way of a plurality of load resistors of the differential inverter amplifier that are electrically coupled between the p-type channel metal oxide semiconductor current source and the n-type channel metal oxide semiconductor current source; and

limiting output swing and minimizing common mode disturbances by use of a plurality of diode-connected metal oxide semiconductor clamps of the differential inverter amplifier that are electrically coupled between the p-type channel metal oxide semiconductor current source and the n-type channel metal oxide semiconductor current source.

8. The method of claim 7 further comprising improving bandwidth and minimizing common mode feedback control by way of a differential resistive load.

9. The method of claim 8 wherein the p-type channel metal oxide semiconductor current source has a voltage vdd.

10. The method of claim 9 wherein the common mode voltage is equal to vdd/2.

11. A differential inverter amplifier for use in a circuit assembly including first and second current sources, said differential inverter amplifier, comprising:

a plurality of load resistors configured to enable optimization of gain and bandwidth; and

a plurality of diode-connected metal oxide semiconductor clamps configured to limit output swing and minimize common mode disturbances independent of the plurality of load resistors.

12. The differential inverter amplifier of claim 11 wherein the first current source is a positive channel metal oxide semiconductor current source.

13. The differential inverter amplifier of claim 12 wherein the second current source is a negative channel metal oxide semiconductor current source.

14. The differential inverter amplifier of claim 13 wherein the circuit further includes a plurality of load resistors configured to provide a common mode voltage.

15. The differential inverter amplifier of claim 14 wherein the circuit further includes a differential resistive load to improve bandwidth and minimize common mode feedback control.