

Description**Field of the invention**

5 This invention relates in general to a BICMOS circuit and, more particular, to an on-chip voltage source and output driver circuit having high input impedance and high output current drive capability that provides full logic output voltage swing for circuits having submicron dimensions.

Background of the invention

10 In many applications of logic circuits, it is essential that the logic circuit have a suitable fan-out (ability to drive a large number loads) or equivalent capacitive drive capability. In order to provide sufficient current drive to heavy capacitive loads, an output buffer is coupled between the output of the logic circuit and the load which is to be driven. Conventional output driver circuits comprise a transistor amplifier, usually in the form of an emitter follower, which has a low output impedance, thereby providing high drive capability, reduced delay per unit load, and fast switching speed. BICMOS circuits combine CMOS devices having high input impedance, good noise immunity and low static power dissipation, and bipolar output transistors having low output impedance and excellent current drive capability.

20 Monolithically integrated CMOS and BICMOS circuits typically operate with a power supply voltage of 5.0 volts. In the case of BICMOS circuits, the bipolar output device is limited to a range of output voltage swing approximated by the power supply voltage minus two base-emitter voltages. CMOS circuits provide output voltage levels equal to the power supply voltage; however, the output impedance is quite high and the current drive is reduced.

25 In an effort to avoid reliability problems associated with high electric field in the gate-drain region (hot electron effect), CMOS and BICMOS circuits having submicron dimensions typically require a voltage supply not to exceed 3.4 volts. As a consequence, systems designed to operate from a 5.0 volt power supply require modification to accommodate a CMOS or BICMOS circuit with submicron dimensions.

30 US-A-4682054 of Motorola Inc teaches a BICMOS circuit including an upper and lower push-pull transistor output stage for providing high output drive without DC power dissipation and further including MOS transistors forming an inverter for the input stage, while a transmission gate serves to aid the output stage transistors in driving the output to the voltage on the supply voltage terminals.

Thus, what is needed is a BICMOS driver circuit having high input impedance and high output current drive that provides the supply voltage and full logic output voltage swing for the submicron circuitry.

Summary of the invention

35 According to the present invention, a driver circuit is provided as defined in claim 1.

The driver circuit can advantageously be fabricated in BICMOS.

40 It provides the advantage of improved output signal characteristics, high input impedance, and low static power requirements. A voltage source may be provided for submicron circuitry.

The circuit can advantageously provide an output voltage swing substantially as large in magnitude as the voltage source for circuitry having submicron dimensions.

45 In a preferred embodiment, a CMOS transistor inverter is coupled to the voltage divider circuit and the input terminal for inverting the input signal. A complimentary emitter follower circuit is coupled between the first and second supply voltage terminals and to an output terminal for providing a digital output signal. A bias circuit is coupled between the first and second supply voltage terminals and is coupled to both the complimentary emitter follower circuit and the inverter circuit for biasing the complimentary emitter follower circuit in response to the inverted input signal. A current source circuit is coupled between the first and second supply voltage terminals and is coupled to both the bias circuit and the input terminal for sourcing current to the bias circuit in response to the input signal.

Brief Description of the Drawing

55 The single figure is a schematic of the present invention.

Detailed Description of the invention

Systems incorporating monolithically integrated circuits (chips) conventionally have used a 5.0 volt power

supply for powering the chips. Newer chips designed with technology having submicron dimensions typically require a smaller supply voltage than the 5.0 volt chips. This presents a problem when chips requiring a 5.0 supply voltage and chips requiring the smaller supply voltage are used in the same system. The invention described herein overcomes this problem by providing both the lower supply voltage (submicron supply voltages) and a digital output signal having a voltage swing over the full submicron supply voltage in response to an input signal from the 5.0 volt system.

Referring to the single figure, a BICMOS driver circuit in accordance with the present invention is shown which may be manufactured in monolithic integrated circuit form. Diodes 1 and 2 are coupled between supply voltage terminal 3 and output voltage terminal 4, and supply voltage terminal 5 and output voltage terminal 6, respectively, and along with resistor 7 coupled between terminals 4 and 6, comprise a voltage divider for providing a first submicron supply voltage at terminal 4 and a second submicron supply voltage at terminal 6. Diodes 1 and 2 and resistor 7 are typical elements for performing this function and may alternatively comprise any combination of other elements and may be located in areas of the chip remote from the remainder of the circuit of FIG. 1. The voltage typically applied to supply voltage terminals 3 and 5 are 5.0 volts and ground, respectively, and are referred to as V_{DD} and V_{SS} , respectively. The voltage appearing on terminal 4 will be one diode drop below V_{DD} , or approximately 4.2 volts, and the voltage appearing on terminal 6 will be one diode drop above V_{SS} , or approximately 0.8 volts. This results in a voltage potential between terminals 4 and 6 of approximately 3.4 volts.

MOS transistor 8 (P channel) has a source connected to the cathode of diode 1, a drain connected to node 9, and a gate connected to input terminal 11. MOS transistor 12 (N channel) has a drain connected to node 9, a source connected to the anode of diode 2, and a gate connected to input terminal 11. In this particular application, the P channel transistor 8 will not have "body effect" (back-gate bias) to consider when establishing the threshold voltage, since the bulk may be tied to the 4.2 volt supply. In contrast, the N channel transistor 12 will have "body effect" to consider when establishing desired threshold voltage. Transistors 8 and 12 function as an inverter for inverting an input signal on input terminal 11 and providing an inverted input signal at node 9.

NPN transistor 13 has a collector connected to supply voltage 3, an emitter connected to output terminal 14, and a base connected to node 15. Substrate PNP transistor 16 has an emitter connected to output terminal 14, a collector connected to supply voltage 5, and a base connected to node 17. Transistors 13 and 16 source from output terminal 14 and sink current from output terminal 14, respectively, in response to signals appearing on nodes 15 and 17, respectively.

MOS transistor 18 (P channel) has a source connected to supply voltage 3, a drain connected to node 15, and a gate connected to input terminal 11. MOS transistor 19 (N channel) has a drain connected to node 17, a source connected to supply voltage 5, and a gate connected to input terminal 11. Transistors 18 and 19 serve as current sources for bipolar transistors 21 and 22.

NPN transistor 21 has a collector connected to supply voltage terminal 3, an emitter connected to node 17, and a base connected to node 9. Substrate PNP transistor 22 has an emitter connected to node 15, a collector connected to supply voltage 5, and a base connected to node 9. Transistors 21 and 22 drive transistors 13 and 16 in response to the inverted input signal on node 9.

While this circuit operates on 5.0 volts from the system into which it may be incorporated, a submicron supply voltage of 3.4 volts appears between terminals 4 and 6 that may be provided to other circuits (loads) on chip that are manufactured with the submicron technology. Furthermore, the excellent current drive capability at terminal 14 is available over the entire voltage swing of 3.4 volts. When a logical zero is present at input terminal 11, the voltage on output terminal 14 will swing high to a voltage of one ϕ (base-emitter drop of transistor 13) less than the 5.0 volts appearing on terminal 3, or approximately 4.2 volts. For a logical one at input terminal 11, the voltage on output terminal 14 will swing low to a voltage of one ϕ (base-emitter drop of transistor 16) greater than the 0.0 volts appearing on terminal 5, or approximately 0.8 volts. This provides a voltage swing of approximately 3.4 volts, the same as the supply voltage provided by terminals 4 and 6.

When the output at terminal 14 is high (steady state), the emitter current of transistor 21 (I_{21H}) and transistor 22 (I_{22H}) is as follows :

$$\begin{aligned}
 I_{21H} &= \text{Beta}_{19}(\phi_D - V_{T19})^2, \\
 \text{where Beta} &= (u/2)(W/L)C_{ox}', \\
 u/2 &= \text{mobility of transistor 19,} \\
 W/L &= \text{gate width over length,} \\
 C_{ox}' &= \text{capacitance per unit surface area,} \\
 \phi_D &= \text{voltage drop across diodes 1 or 2,} \\
 V_{T19} &= \text{threshold of transistor 19.} \\
 I_{22H} &= (\phi_D - \phi_{22})/R_{18}.
 \end{aligned}$$

where ϕ_{22} = transistor 22 base-emitter voltage,
 R_{18} = on resistance of transistor 18 in linear region.

When the output at terminal 14 is low (steady state), the emitter current of transistor 21 (I_{21L}) and transistor 22 (I_{22L}) is as follows :

I_{21L} = $(\phi_D - \phi_{21})/R_{19}$,
 where ϕ_{21} = transistor 21 base-emitter voltage,
 R_{19} = on resistance of transistor 19 in linear region.
 I_{22L} = $BETA_{18}(\phi_D - V_{T18})^2$,
 where V_{T18} = threshold of transistor 18.

The average current ($I_{13, 16}$) between the emitters of transistors 13 and 16 (where transistors 13 and 21, and 16 and 22, respectively, are matched in accordance with current mirror techniques) is as follows :

$$(I_{13, 16}) = \frac{\sqrt{I_{21H}} (I_{22H}) + \sqrt{I_{21L}} (I_{22L})}{2}$$

Therefore, the average current from V_{DD} less the current through resistor 7 is as follows :

$$I_T = \frac{I_{21H} + I_{22H} + I_{21L} + I_{22L}}{2} + I_{13, 16}$$

Furthermore, the current (I_7) through resistor 7 may be expressed as follows :

I_7 = $(V_{DD} - 2\phi_D)R_7$,
 where R_7 = resistance of resistor 7,
 ϕ_D = $(kT/q)\ln(I_D/I_S)$,
 k = Boltzmann's constant,
 T = absolute temperature,
 q = electronic charge,
 I_S = saturation current.

Therefore, it is seen that ϕ_D may be adjusted by setting the current through resistor 7 (I_7), thereby setting I_T .

As a result, the average current from V_{DD} is as follows :
 $I_{DD} = nI_T + I_7$,

where n = number of output driver circuits on a chip.

It may be noted from the above discussion that output bipolar transistors 13 and 16 have there high conduction states controlled by the opposite polarity MOS transistors 18 and 19 and simultaneously have their low conduction states controlled by the opposite polarity bipolar input transistors 21 and 22. This design greatly reduces any power supply glitch current flowing through transistors 13 and 16 during the switching action and thereby enhances switching speed. Furthermore, bipolar transistors 13, 16, 21, and 22 are operated as emitter followers and therefore require no process steps for minimizing device collector-substrate capacitance.

By now it should be appreciated that there has been provided an output driver circuit having high input impedance and high output current drive with low static power dissipation that provides supply voltages and full logic output voltage swing for circuits having submicron dimensions.

Claims

1. A driver circuit, comprising :
 an input terminal (11) coupled for receiving a digital input signal ;
 an output terminal (14) ;



where $\phi_{22} =$ transistor 22 base-emitter voltage,
 $R_{18} =$ on resistance of transistor 18 in linear region.

When the output at terminal 14 is low (steady state), the emitter current of transistor 21 (I_{21L}) and transistor 22 (I_{22L}) is as follows :

$I_{21L} = (\phi_D - \phi_{21})/R_{19}$,
 where $\phi_{21} =$ transistor 21 base-emitter voltage,
 $R_{19} =$ on resistance of transistor 19 in linear region.
 $I_{22L} = \text{BETA}_{18}(\phi_D - V_{T18})^2$,
 where $V_{T18} =$ threshold of transistor 18.

The average current ($I_{13, 16}$) between the emitters of transistors 13 and 16 (where transistors 13 and 21, and 16 and 22, respectively, are matched in accordance with current mirror techniques) is as follows :

$$(I_{13, 16}) = \frac{\sqrt{(I_{21H})(I_{22H})} + \sqrt{(I_{21L})(I_{22L})}}{2}$$

Therefore, the average current from V_{DD} less the current through resistor 7 is as follows :

$$I_T = \frac{I_{21H} + I_{22H} + I_{21L} + I_{22L}}{2} + I_{13, 16}$$

Furthermore, the current (I_7) through resistor 7 may be expressed as follows :

$I_7 = (V_{DD} - 2\phi_D)R_7$,
 where $R_7 =$ resistance of resistor 7,
 $\phi_D = (kT/q)\ln(I_D/I_S)$,
 $k =$ Boltzmann's constant,
 $T =$ absolute temperature,
 $q =$ electronic charge,
 $I_S =$ saturation current.

Therefore, it is seen that ϕ_D may be adjusted by setting the current through resistor 7 (I_7), thereby setting I_T .

As a result, the average current from V_{DD} is as follows :

$$I_{DD} = nI_T + I_7,$$

where $n =$ number of output driver circuits on a chip.

It may be noted from the above discussion that output bipolar transistors 13 and 16 have there high conduction states controlled by the opposite polarity MOS transistors 18 and 19 and simultaneously have their low conduction states controlled by the opposite polarity bipolar input transistors 21 and 22. This design greatly reduces any power supply glitch current flowing through transistors 13 and 16 during the switching action and thereby enhances switching speed. Furthermore, bipolar transistors 13, 16, 21, and 22 are operated as emitter followers and therefore require no process steps for minimizing device collector-substrate capacitance.

By now it should be appreciated that there has been provided an output driver circuit having high input impedance and high output current drive with low static power dissipation that provides supply voltages and full logic output voltage swing for circuits having submicron dimensions.

Claims

1. A driver circuit, comprising :
 an input terminal (11) coupled for receiving a digital input signal ;
 an output terminal (14) ;



- a first supply voltage terminal (3) coupled for receiving a first supply voltage ;
 a second supply voltage terminal (5) coupled for receiving a second supply voltage ;
 a third supply voltage terminal (4) ;
 a fourth supply voltage terminal (6) ;
- 5 first means (8, 12) coupled between said third and fourth supply voltage terminals (4, 6) and to said input terminal (11) for inverting said digital input signal ;
 second means (13, 16) coupled between said first and second supply voltage terminals (3, 5) and to said output terminal (14) for providing a digital output signal having an upper voltage swing substantially equal in magnitude to said third supply voltage and a lower voltage swing substantially equal in magnitude to said fourth supply voltage ; characterized by
- 10 third means (1, 2) coupled between said first and second supply voltage terminals (3, 5) for dividing the voltage difference between said first and second supply voltages and providing third and fourth supply voltages at said third and fourth supply voltage terminals (4, 6), respectively ;
 fourth means (21, 22) coupled between said first and second supply voltage terminals (3, 5) and coupled to both said second means (13, 16) and said first means (8, 12) for biasing said second means in response to said inverted digital input signal ; and
 fifth means (18, 19) coupled between said first and second supply voltage terminals (3, 5) and coupled to both said fourth means (21, 22) and said input terminal (11) for sourcing current to said fourth means in response to said digital input signal, the magnitude of the current being proportional to the magnitude of said digital input signal.
- 20 2. The driver circuit according to claim 1 wherein said second means comprises a pair of complimentary push pull bipolar transistors (13, 16) having their emitters coupled to said output terminal (14), their collectors coupled to said first and second supply voltage terminals (3, 5), respectively, and their bases coupled to said fourth means (21, 22).
- 25 3. The driver circuit according to claim 2 wherein said fourth means comprises complimentary bipolar transistors (21, 22) having their collectors coupled to said first and second supply voltage terminals (3, 5), respectively, their emitters coupled to the bases of said pair of complimentary push-pull bipolar transistors (13, 16), respectively, and their bases coupled for receiving said inverted digital input signal.
- 30 4. The driver circuit according to claim 3 wherein said first means comprises first complimentary MOS transistors (8, 12) having their sources coupled to said first and second supply voltage terminals (3, 5), respectively, their drains coupled together for providing said inverted digital input signal, and their gates coupled to said input terminal (11).
5. The driver circuit according to claim 4 wherein said fifth means comprises second complimentary MOS transistors (18, 19) having their sources coupled to said first and second supply voltage terminals (3, 5), respectively, their drains coupled to the emitters of said complimentary bipolar transistors, respectively, and their gates coupled to said input terminal (11).
- 35

Patentansprüche

- 40 1. Treiberschaltung
 mit einer zum Empfang eines digitalen Eingangssignals angeschlossenen Eingangsklemme (11),
 mit einer Ausgangsklemme (14),
 mit einer ersten zur Aufnahme einer ersten Ladespannung angeschlossenen Spannungsklemme (3),
 45 mit einer zweiten zur Aufnahme einer zweiten Ladespannung angeschlossenen Spannungsklemme (5),
 mit einer dritten Ladespannungsklemme (4),
 mit einer vierten Ladespannungsklemme (6),
 mit einer ersten Vorrichtung (8, 12), die zur Invertierung des digitalen Eingangssignals zwischen der dritten und vierten Ladespannungsklemme (4, 6) an der Eingangsklemme (11) angeschlossen ist,
 50 mit einer zweiten Vorrichtung (13, 16), die zwischen der ersten und zweiten Ladespannungsklemme (3, 5) an der Ausgangsklemme (14) angeschlossen ist, um ein digitales Signal abzugeben, dessen oberer Spannungsaus-
 schlag im wesentlichen mit der dritten Ladespannung und dessen unterer Spannungsaus-
 schlag im wesentlichen mit der vierten Ladespannung grössengleich ist, dadurch gekennzeichnet,
 daß eine dritte Vorrichtung (1, 2) zwischen der ersten und zweiten Ladespannungsklemme (3, 5) an-
 55 geschlossen ist, um die Spannungsdifferenz zwischen der ersten und zweiten Ladespannung zu teilen bzw.
 die dritte und vierte Ladespannung an der dritten bzw. vierten Ladespannungsklemme (4, 6) vorzusehen,
 daß eine vierte Vorrichtung (21, 22) zwischen der ersten und zweiten Ladespannungsklemme (3, 5) an
 der zweiten Vorrichtung (13, 16) und der ersten Vorrichtung (8, 12) angeschlossen ist, um in Abhängigkeit



5 von dem invertierten, digitalen Eingangssignal der zweiten Vorrichtung eine Vorspannung zu erteilen, und daß eine fünfte Vorrichtung (18, 19) zwischen der ersten und zweiten Ladespannungsklemme (3, 5) sowohl an der vierten Vorrichtung (21, 22) als auch an der Eingangsklemme (11) angeschlossen ist, um in Abhängigkeit von dem digitalen Eingangssignal der vierten Vorrichtung Strom zuzuführen, dessen Größe der Größe des digitalen Eingangssignals proportional ist.

2. Treiberschaltung gemäß Anspruch 1, bei der die zweite Vorrichtung zwei bipolare, komplementäre Gegentakt-Transistoren (13, 16) enthält, deren Emittter an der Ausgangsklemme (14), deren Kollektoren an der ersten bzw. zweiten Ladespannungsklemme (3, 5) und deren Basen an der vierten Vorrichtung (21, 22) angeschlossen sind.

10 3. Treiberschaltung gemäß Anspruch 2, bei der die vierte Vorrichtung bipolare, komplementäre Transistoren (21, 22) enthält, deren Kollektoren an der ersten bzw. zweiten Ladespannungsklemme (3, 5), deren Emittter jeweils an den Basen der beiden bipolaren, komplementären Gegentakt-Transistoren (13, 16) und deren Basen zur Aufnahme des invertierten, digitalen Eingangssignals angeschlossen sind.

15 4. Treiberschaltung gemäß Anspruch 3, bei der die erste Vorrichtung erste komplementäre MOS-Transistoren (8, 12) enthält, deren Quallelektroden mit der ersten bzw. zweiten Ladespannungsklemme (3, 5) verbunden sind, deren Zuelektroden zur Erzielung des invertierten, digitalen Eingangssignals zusammengeschlossen sind, und deren Torelektroden mit der Eingangsklemme (11) verbunden sind.

20 5. Treiberschaltung gemäß Anspruch 4, bei der die fünfte Vorrichtung zweite komplementäre MOS-Transistoren (18, 19) enthält, deren Quallelektroden an der ersten bzw. zweiten Ladespannungsquelle (3, 5), deren Zuelektroden jeweils an den Emitttern der bipolaren, komplementären Transistoren und deren Torelektroden an der Eingangsklemme (11) angeschlossen sind.

Revendications

25

1. Circuit d'excitation comprenant :

une borne d'entrée (11) couplée de façon à recevoir un signal d'entrée numérique ;

une borne de sortie (14) ;

30 une première borne de tension d'alimentation électrique (3) couplée de façon à recevoir une première tension d'alimentation ;

une deuxième borne de tension d'alimentation électrique (5) couplée de façon à recevoir une deuxième tension d'alimentation ;

une troisième borne de tension d'alimentation électrique (4) destinée à produire une troisième tension d'alimentation ;

35 une quatrième borne de tension d'alimentation électrique (6) destinée à produire une quatrième tension d'alimentation ;

un premier moyen (8, 12) couplé entre lesdites troisième et quatrième bornes de tension d'alimentation (4, 6) et à ladite borne d'entrée (11) afin d'inverser ledit signal d'entrée numérique ;

40 un deuxième moyen (13, 16) couplé entre lesdites première et deuxième bornes de tension d'alimentation (3, 5) et à ladite borne de sortie (14) afin de produire un signal de sortie numérique possédant une excursion de tension supérieure qui est sensiblement égale, en amplitude, à ladite troisième tension d'alimentation et une excursion de tension inférieure qui est sensiblement égale, en amplitude, à ladite quatrième tension d'alimentation ; caractérisé par :

45 un troisième moyen (1, 2) couplé entre lesdites première et deuxième bornes de tension d'alimentation (3, 5) afin de diviser la différence de tension entre lesdites première et deuxième tensions d'alimentation et de produire respectivement lesdites troisième et quatrième tensions d'alimentation sur lesdites troisième et quatrième bornes de tension d'alimentation (4, 6) ;

50 un quatrième moyen (21, 22) couplé entre lesdites première et deuxième bornes de tension d'alimentation (3, 5) et couplé à la fois audit deuxième moyen (13, 16) et audit premier moyen (8, 12) afin de polariser ledit deuxième moyen en réponse audit signal d'entrée numérique inversé ; et

un cinquième moyen (18, 19) couplé entre lesdites première et deuxième bornes de tension d'alimentation (3, 5) et couplé à la fois audit quatrième moyen (21, 22) et à ladite borne d'entrée (11) afin de faire fonction de source de courant pour ledit quatrième moyen en réponse audit signal d'entrée numérique, l'intensité du courant étant proportionnelle à l'amplitude dudit signal d'entrée numérique.

55

2. Circuit d'excitation selon la revendication 1, où ledit deuxième moyen comprend une paire de transistors bipolaires push-pull complémentaires (13, 16) dont les émetteurs sont couplés à ladite borne de sortie (14), les collecteurs sont couplés respectivement auxdites première et deuxième bornes de tension d'alimentation (3, 5), et les bases sont couplées audit quatrième moyen (21, 22).



3. Circuit d'excitation selon la revendication 2, où ledit quatrième moyen comprend des transistors bipolaires complémentaires (21, 22) dont les collecteurs sont respectivement couplés auxdites première et deuxième bornes de tension d'alimentation (3, 5), les émetteurs sont respectivement couplés aux bases de ladite paire de transistors bipolaires push-pull complémentaires (13, 16), et les bases sont couplées de façon à recevoir ledit signal d'entrée numérique inversé.

4. Circuit d'excitation selon la revendication 3, où ledit premier moyen comprend des premiers transistors MOS complémentaires (8, 12) dont les sources sont respectivement couplées auxdites première et deuxième bornes de tension d'alimentation (3, 5), les drains sont couplés ensemble de façon à produire ledit signal d'entrée numérique inversé, et les grilles sont couplées à ladite borne d'entrée (11).

5. Circuit d'excitation selon la revendication 4, où ledit cinquième moyen comprend des deuxièmes transistors MOS complémentaires (18, 19) dont les sources sont respectivement couplées auxdites première et deuxième bornes de tension d'alimentation (3, 5), les drains sont respectivement couplés aux émetteurs desdits transistors bipolaires complémentaires, et les grilles sont couplées à ladite borne d'entrée (11).

15

20

25

30

35

40

45

50

55