Method for manufacturing a high-resistivity semiconductor-on-insulator substrate

The invention relates to a method for manufacturing a high-resistivity (HR) semiconductor-on-insulator (SOI) substrate, to a high-resistivity semiconductor-on-insulator substrate obtained via such a method and to a semiconductor device.

Complex semiconductor substrates may be manufactured by combining two or more layers. One class of such engineered substrates are semiconductor-on-insulator substrates, wherein a top semiconductor layer is formed over a carrier substrate with a dielectric layer in between. For the top semiconductor layer and the carrier substrate, usually silicon is used and the dielectric layer is usually an oxide layer, typically a silicon oxide.

Especially so-called high-resistivity (HR) substrates are currently investigated for use for radiofrequency (RF) applications due to their reduced substrate loss and coupling.

It has been found, however, that between the high-resistivity substrate and the thin dielectric layer, a so-called parasitic conduction layer can be formed, compromising the RF performance, particularly the expected benefits in substrate loss and coupling.

Various solutions for this problem have been proposed. For instance, a continuous trap-rich layer under the buried oxide layer has been suggested ("Identification of RF Harmonic Distortion on Si Substrates and its Reduction Using a Trap-Rich Layer" by Kerr, et al., IEEE, 2008). This single trap-rich layer, however, has negative effects connected to the back gate formation process. Particularly, due to a larger lateral doping diffusion and a high interface trap density in the back gate a problem of variability and, thus, of reliability of the obtained structure may arise.

Furthermore, from US 8,492,868, a method of forming an integrated circuit structure is known, wherein a silicon substrate layer is formed having trench structures and an ion impurity implant. An insulator layer is then positioned on and contacts the silicon substrate layer, wherein the insulator layer also fills the trench structures. A circuitry layer is then positioned on and contacts the buried insulator layer. The ion impurity implant allows avoiding the above-mentioned parasitic conduction layer. Since this method first forms trenches in the substrate and then the buried oxide layer on the substrate, however, the subsequent formation of the semiconductor layer on the buried oxide layer may be complicated. Furthermore, this teaching does not account for the co-integration of, for instance, digital circuits.

Embodiments of the present invention provide an improved method for manufacturing a high-resistivity semiconductor-on-insulator substrate, a correspondingly

improved high-resistivity semiconductor-on-insulator substrate, and an improved semiconductor device comprising such a high-resistivity semiconductor-on-insulator substrate.

According to an aspect of the present invention, there is provided method for manufacturing a high-resistivity semiconductor-on-insulator substrate comprising the steps of: forming a dielectric layer and a semiconductor layer over a high-resistivity substrate, such that the dielectric layer is arranged between the high-resistivity substrate and the semiconductor layer; forming a hard mask or resist over the semiconductor layer, wherein the hard mask or resist has at least one opening at a predetermined position; forming at least one doped region in the high-resistivity substrate by ion implantation of an impurity element through the at least one opening of the hard mask or resist, the semiconductor layer and the dielectric layer; removing the hard mask or resist; forming a radiofrequency circuit at least one of in and on the semiconductor layer, the radiofrequency circuit at least partially overlapping the at least one doped region in the high-resistivity substrate; and forming at least one of an analog circuit and a digital circuit respectively at least one of in and on the semiconductor layer, the at least one of the analog circuit and the digital circuit being formed in an area not overlapping the doped region in the high-resistivity semiconductor-on-insulator substrate.

By using a local implantation through the semiconductor layer and the dielectric layer using a hard mask or resist, it is possible to form a localized trap-rich region in the high-resistivity substrate. In particular, it is possible to form the trap-rich region under the RF circuit only. This trap-rich region can avoid the above-mentioned parasitic conduction layer below the RF circuit, so that the RF performance is not diminished. Additional analog or digital portions of a circuit may be provided, below which, however, no trap-rich region is formed. This can be particularly beneficial as the digital/analog portions often require an efficient back biasing. For achieving such an efficient back biasing, a trap-rich layer below the digital/analog portions would have disadvantages.

Embodiments of the present invention, thus, also provide the use of a localized doped layer in a high-resistivity semiconductor-on-insulator substrate below an RF circuit to avoid formation of a parasitic conduction layer between the high-resistivity substrate and the dielectric layer in the region below the RF circuit, wherein the localized doped layer is formed by ion implantation of an impurity element through an opening of a hard mask or resist, through the semiconductor layer and through the dielectric layer.

Advantageous embodiments will now be described in combination with the enclosed figures.

FIGURE 1 shows a simplified flowchart of the method according to the invention;

FIGURE 2 illustrates an intermediate step of the manufacturing method according to the invention;

FIGURE 3 illustrates another intermediate step of the method according to the invention;

FIGURE 4 illustrates further steps of the method according to the invention;

FIGURE 5 illustrates an exemplary semiconductor substrate according to the invention; and

FIGURE 6 illustrates an exemplary semiconductor device according to the invention.

Claims:

1. A method for manufacturing a high-resistivity semiconductor-on-insulator substrate comprising the steps of:

a) forming a dielectric layer and a semiconductor layer over a high-resistivity substrate, such that the dielectric layer is arranged between the high-resistivity substrate and the semiconductor layer;

b) forming a hard mask or resist over the semiconductor layer, wherein the hard mask or resist has at least one opening at a predetermined position;

c) forming at least one doped region in the high-resistivity substrate by ion implantation of an impurity element through the at least one opening of the hard mask or resist, the semiconductor layer and the dielectric layer;

d) removing the hard mask or resist;

e) forming a radiofrequency circuit at least one of in and on the semiconductor layer, the radiofrequency circuit at least partially overlapping the at least one doped region in the high-resistivity substrate; and

f) forming at least one of an analog circuit and a digital circuit respectively at least one of in and on the semiconductor layer, the at least one of the analog circuit and the digital circuit being formed in an area not overlapping the doped region in the high-resistivity semiconductor-on-insulator substrate.

2. The method according to claim 1, wherein the impurity element implanted by ion implantation in step c) comprises at least one of C, Ge, O, Si, Ar, Mo and F.

3. The method according to claim 1, wherein the high-resistivity substrate comprises silicon.

4. The method according to claim 3, wherein the high-resistivity substrate comprises polycrystalline silicon.

5. The method according to claim 3, wherein the high-resistivity substrate comprises single crystal silicon.

6. The method according to claim 1, wherein the high-resistivity substrate comprises polycrystalline silicon.

7. The method according to claim 1, wherein the high-resistivity substrate comprises single crystal silicon.

8. The method according to claim 1, wherein the dielectric layer is a buried oxide layer.

9. The method according to claim 1, wherein the semiconductor layer comprises silicon.

10. The high-resistivity semiconductor-on-insulator substrate obtained by the method according to claim 1.