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[Continued on next page]

- (54) Title:** APPARATUSES AND METHODS FOR VARIABLE LATENCY MEMORY OPERATIONS

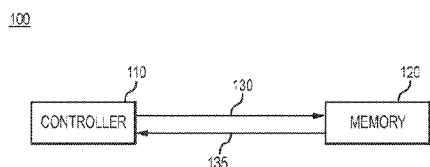


FIGURE 1A

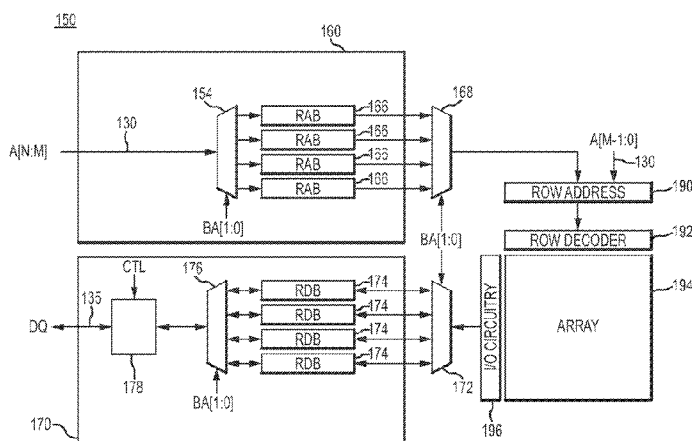


FIGURE 1B

(57) Abstract: Apparatuses and methods for variable latency memory operations are disclosed herein. An example apparatus may include a memory configured to receive an activate command indicative of a type of a command during a first addressing phase and to receive the command during a second addressing phase. The memory may further be configured to provide information indicating that the memory is not available to perform a command responsive, at least in part, to receiving the command during a variable latency period and to provide information indicating that the memory is available to perform a command responsive, at least in part, to receiving the command after the variable latency period.



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